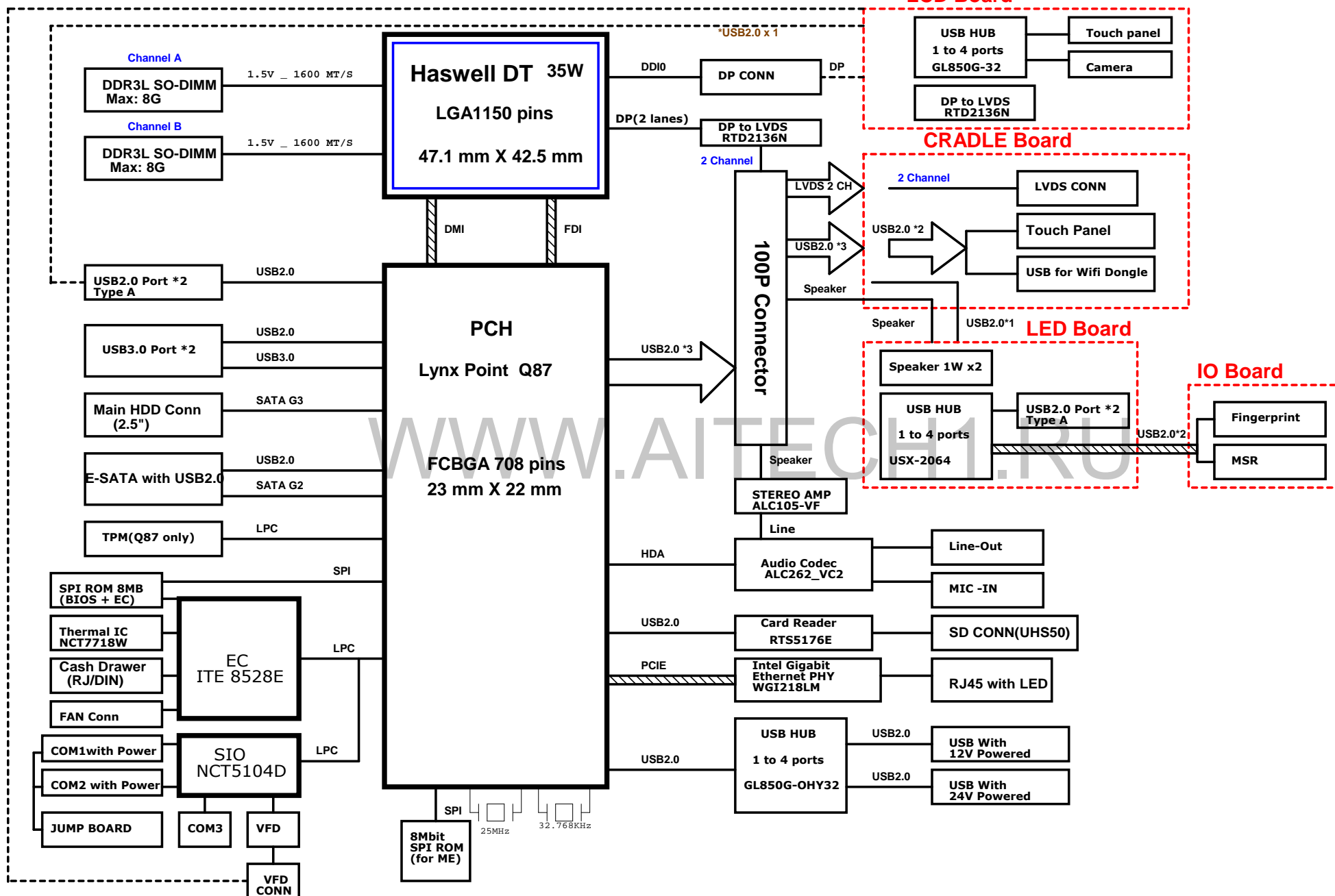


# POS High End BLOCK DIAGRAM



\*Change jumper pins, COM1/COM2 can receive either RI(default) or power supply(+5V/+12V, 500mA max)

USB 2.0	Port Assignment	xHCI Port	EHCI Port	OC# Default
USBP0	External USB3.0 port	0	0	OC0#
USBP1	External USB3.0 port <b>Debug</b>	1	1	
USBP2	External port(USB2 CONN)	2	2	OC1#
USBP3	External port(USB2 CONN)	3	3	
USBP4	USB2 HUB for MB ( <b>H81 ONLY</b> )	8	4	OC2#
USBP5	eSATA	9	5	
USBP6	USB2.0 with 12V ( <b>Q87 ONLY</b> )	12	6	OC3#
USBP7	USB2.0 with 24V ( <b>Q87 ONLY</b> )	13	7	
USBP8	Card Reader	4	8	OC4#
USBP9	Touch Panel (DB) <b>Debug</b>	5	9	
USBP10	Wifi Dongle (DB)	6	10	OC5#
USBP11	USB2 HUB for LED board (BD)	7	11	
USBP12	<b>NA (H81 don't support)</b>	10	12	OC6#
USBP13	<b>NA (H81 don't support)</b>	11	13	

PS : OC7# Default not used (486712\_486712\_HSW\_6L\_AIO\_PDG\_r2\_1\_1 (PG173))

USB2 HUB	Port Assignment (H81 ONLY)
USBP1	USB2.0 with 12V
USBP2	USB2.0 with 24V
USBP3	NA
USBP4	NA

USB 3.0	Port Assignment
USBP1	External port (USB3 CONN)
USBP2	External port (USB3 CONN)
USBP3	NA
USBP4	NA

PCIE Master	Port Assignment
PCIE 3	LAN with Intel Gigabit
PCIE 4	NA
PCIE 5	NA
PCIE 6	NA

Display Port	Port Assignment
DDIC	DP
DDID	RTD2136N DP transfer to LVDS

SATA Master	Port Assignment
SATA0	SATA HDD (Main) G3
SATA1	e-SATA CONN G2.
SATA2	NA
SATA3	NA
PCIe1/SATA4	NA
PCIe2/SATA5	NA

Table 1-3. Intel® 8 Series/C220 Series Chipset Family PCH SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
Q87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	USB 3.0 Port 5	USB 3.0 Port 6	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4	SATA 6Gb/s Port 5	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
H81	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	NA	NA	SATA 3Gb/s Port 4	SATA 3Gb/s Port 5	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	NA	NA

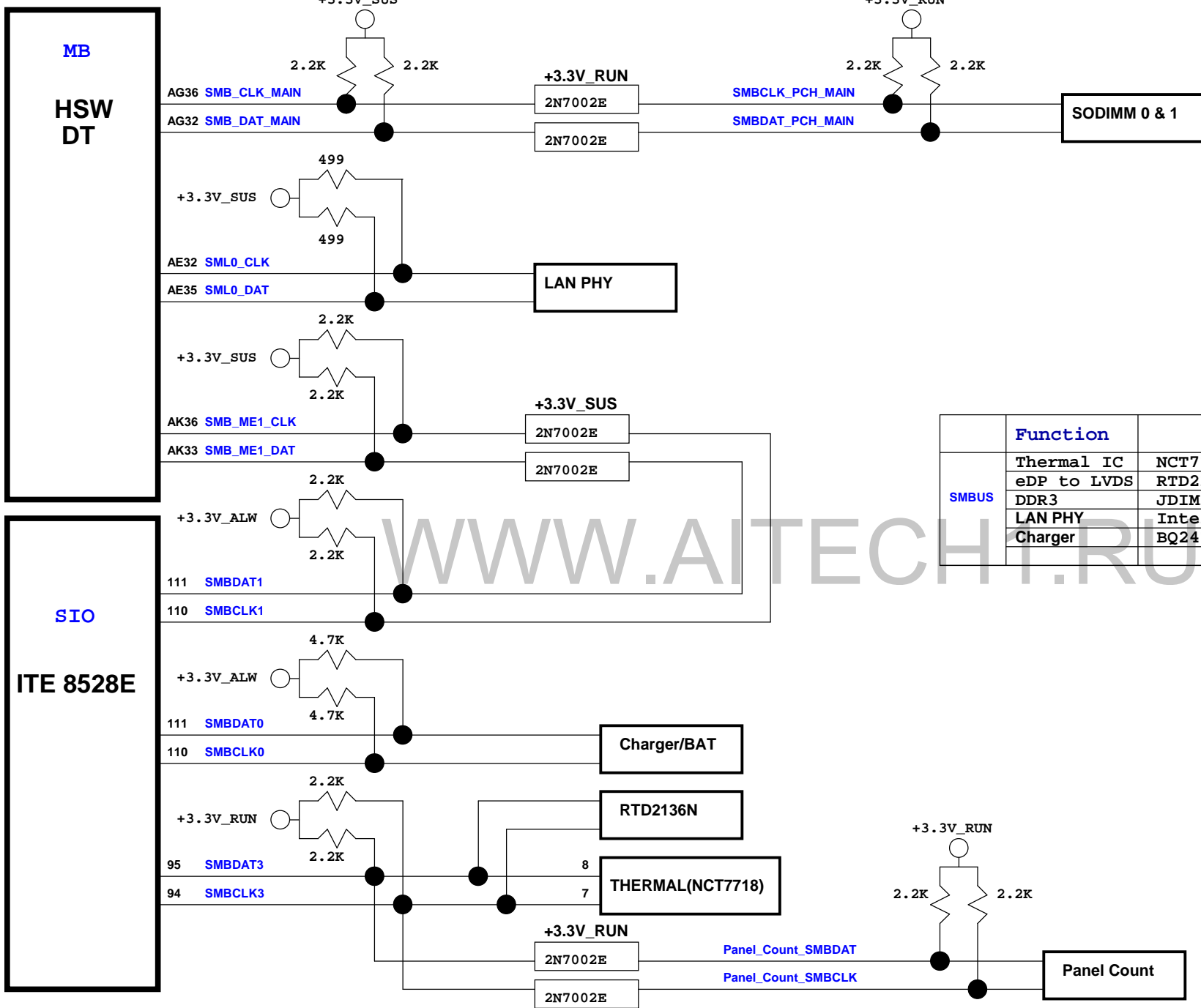
NOTE : (For H81)

1. USB 2.0 ports 6,7,12 and 13 are disabled on 10 port SKUs.
2. Only USB 3.0 ports 1 and 2 are enabled.
3. SATA ports 2 and 3 are disabled on 4 port SKUs.



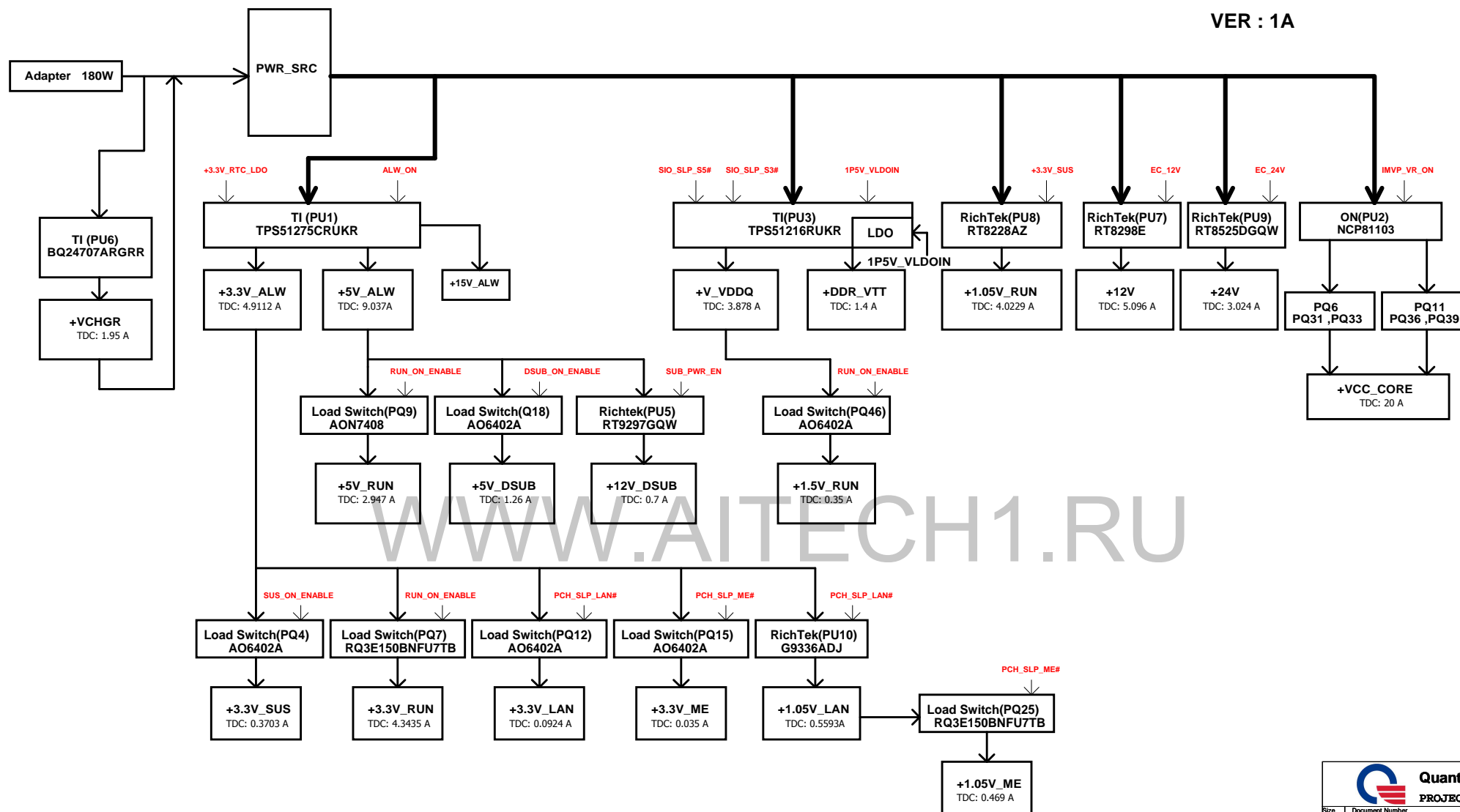
**Quanta Computer Inc.**

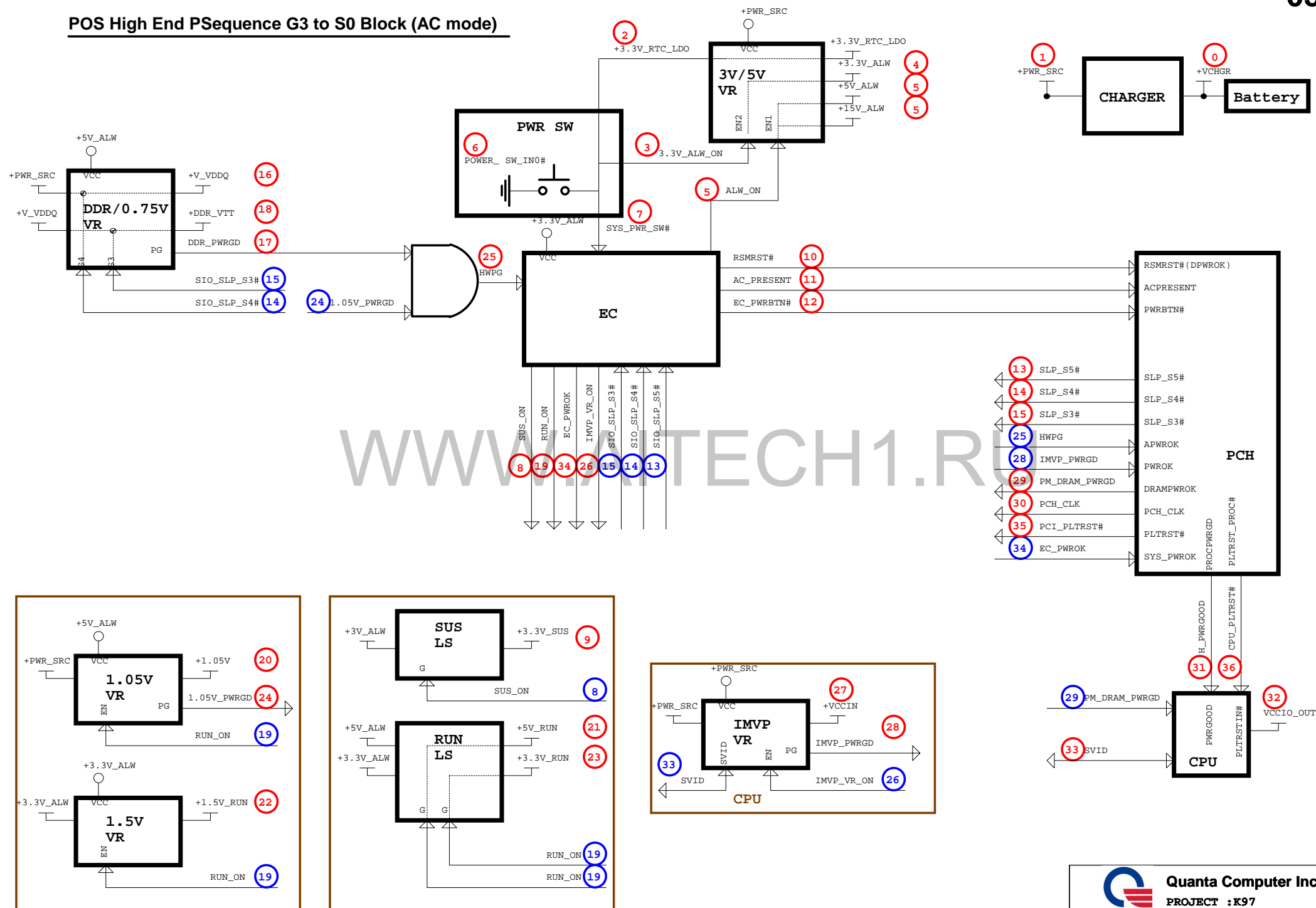
**PROJECT : K97**



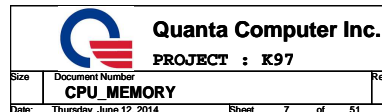
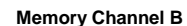
	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	eDP to LVDS	RTD2132R-CG	0xA8
	DDR3	JDIM1A	0xA0h
	LAN PHY	Intel I217	0xC8h
	Charger	BQ24707BGRR	0X12h

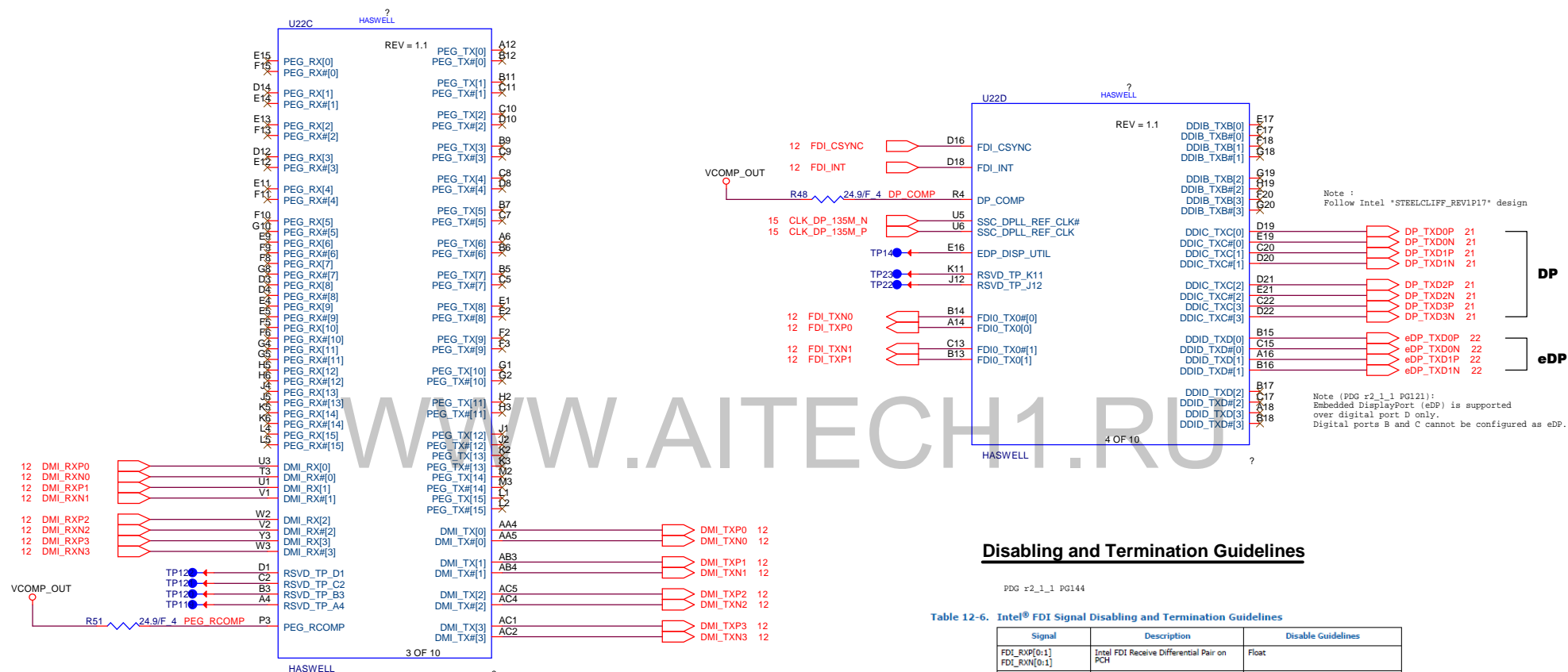
VER : 1A











## Disabling and Termination Guidelines

PDG r2\_l\_1 PG144

Table 12-6. Intel® FDI Signal Disabling and Termination Guidelines

Signal	Description	Disable Guidelines
FDL_RXP[0:1] FDL_RXN[0:1]	Intel FDI Receive Differential Pair on PCH	Float
FDL_TXP[0:1] FDL_TXN[0:1]	Intel FDI Transmit Differential Pair on Processor	Float
FDI_CS_SYNC	Intel FDI Composite Sync	Connect between Processor and PCH
FDI_INT	Intel FDI Hot Plug Interrupt	Connect between Processor and PCH
FDI_RCOMP	FDI Resistor Compensation	Float
FDI_REF	FDI Reference Voltage	Float

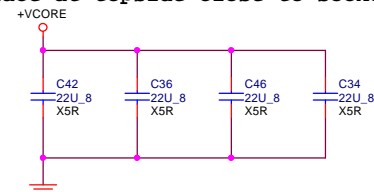
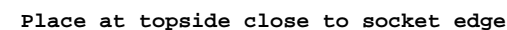


**Quanta Computer Inc.**

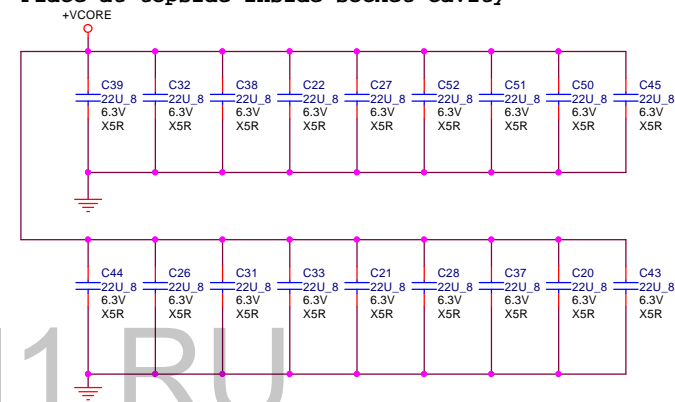
**PROJECT : K97**





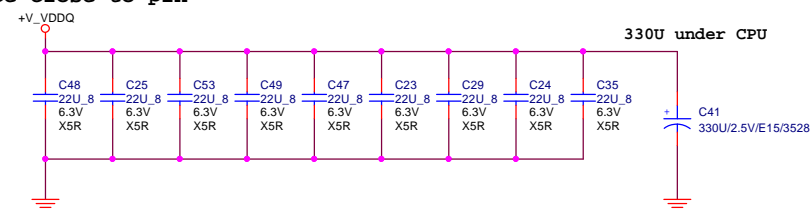


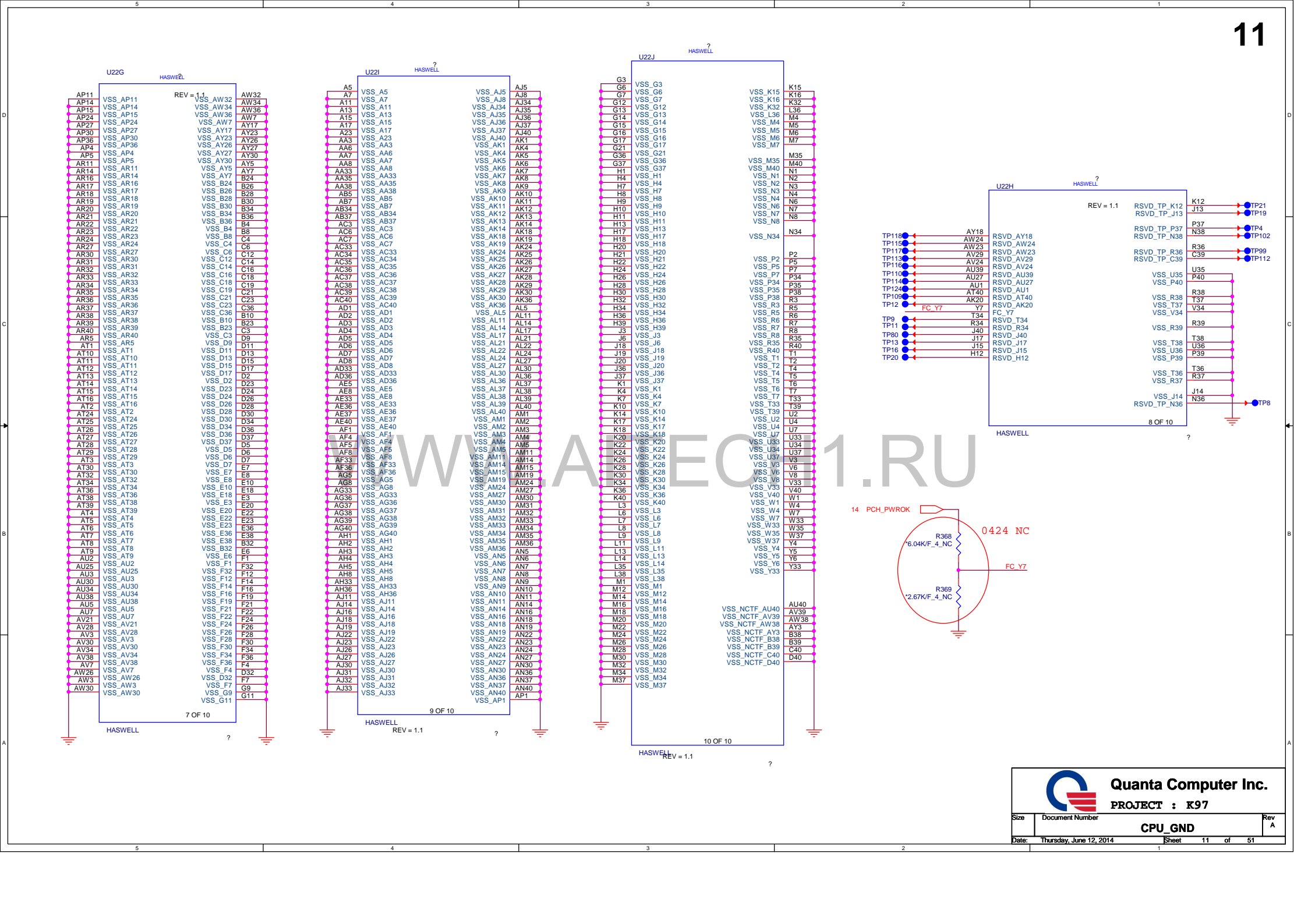
Place at topside inside socket cavity

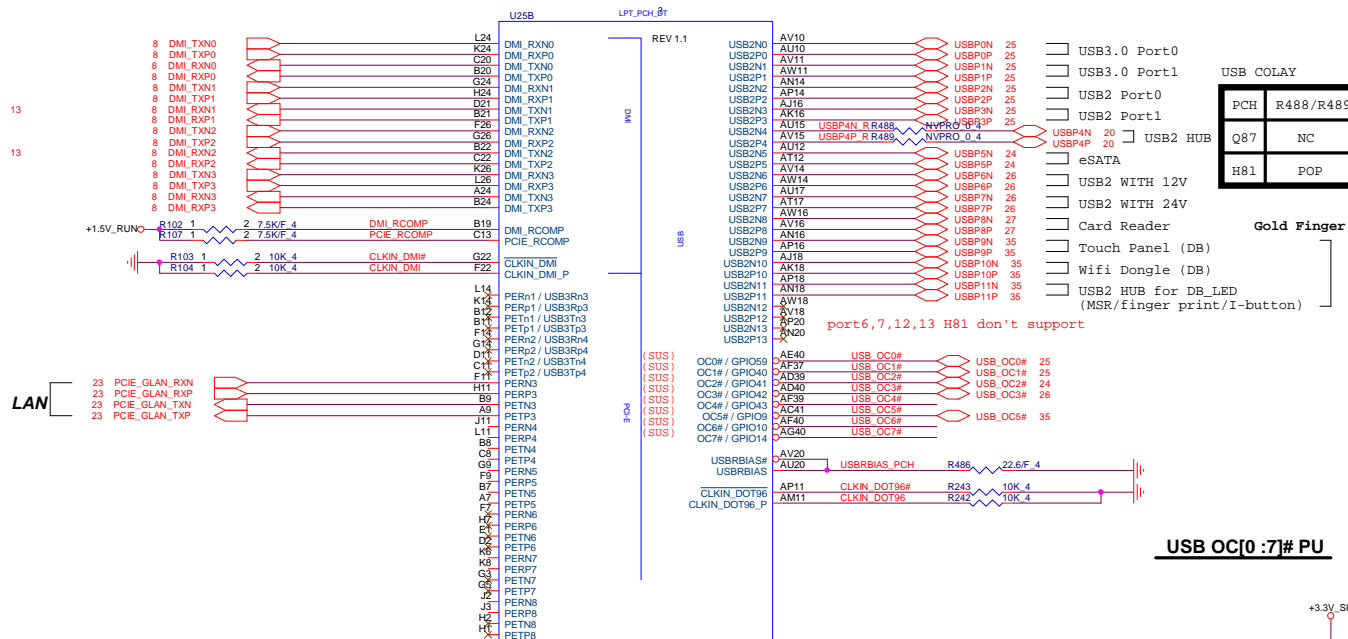
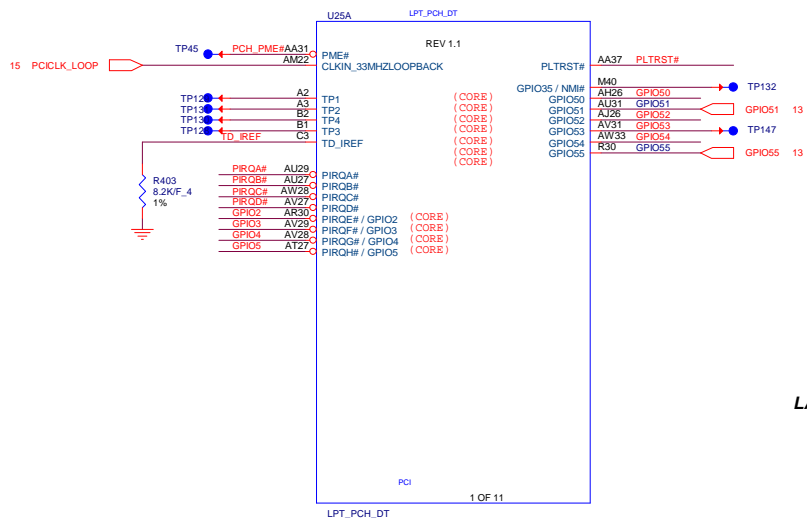


VCCQ POWER NOTE:  
4.5A MAX

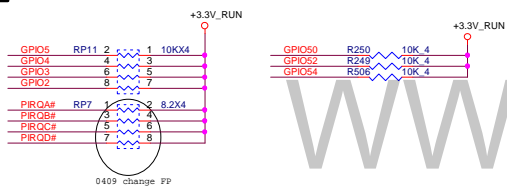
Place close to pin



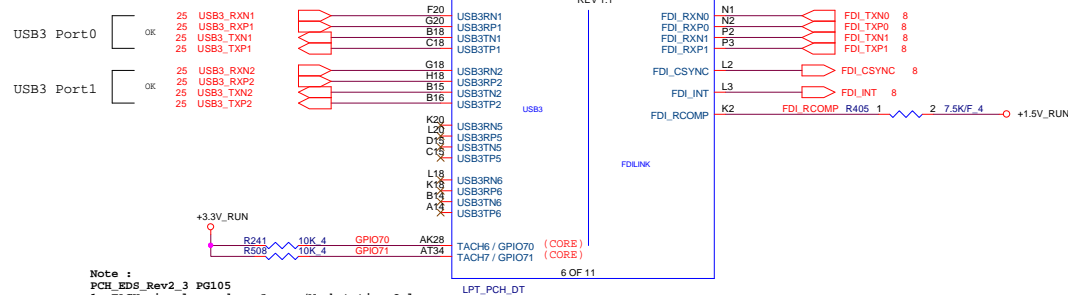
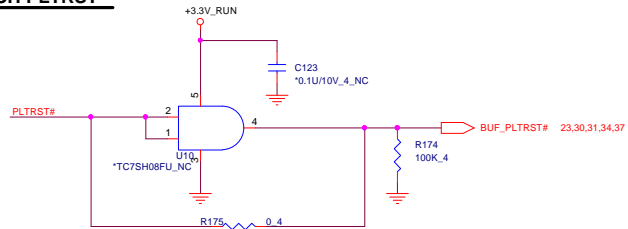




## PCI PULL-UPS



**PCH PLTRST**



Note :

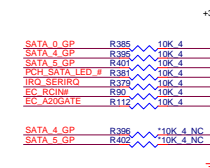
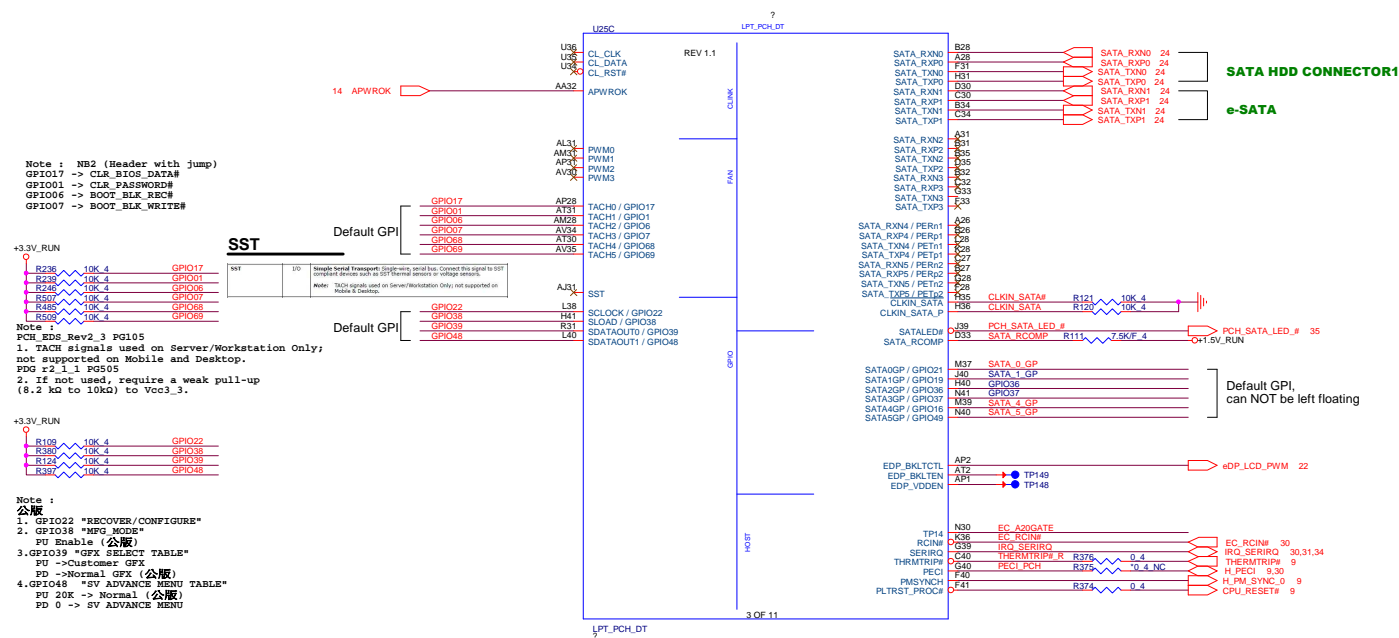
FCH\_EDS\_Rev2\_3 PG105

1. TACH signals used on Server/Workstation Only;  
not supported on Mobile and Desktop.

PDG r2\_1\_1 PG505

2. If not used, require a weak pull-up  
(8.2 kΩ to 10kΩ) to Vcc3.3.









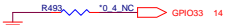




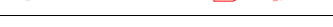

PCH	H81/U25	Q87
vPRO	NC	AJSR1730T00 /U25 IC CTRL(708P)DH82Q87 SR173(FCBGA)
nonvPRO	AJSR1770T00 /U25 IC CTRL(708P)DH82H81 SR177(FCBGA)	NC



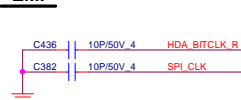
Note :

1. SATA\_4\_GP(GPIO16) CAN BE USE AS PCIE 1/MSATA 4 MUX SELECT IN LPT
2. SATA\_5\_GP(GPIO49)CAN BE USE AS PCIE 2/MSATA 5 MUX SELECT IN LPT

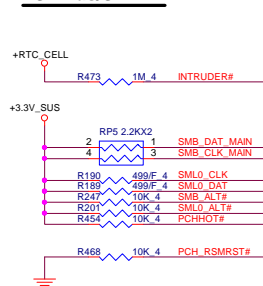
Strap Pin Table (PCH EDS Rev2\_3 PG95)

Pin Name	Strap description	Sampled	Configuration	Note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN0  ACZ_SPKR 14.28												
GPIO53	DMI AC(or AC) - Coupling Mode Reserved	PWROK	weak internal pull up Should not be pull-down	NC												
GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	 GPIO55 12												
INTVRMEN	Integrated VRM Enable	ALWAYS	Should be always pull-up	+RTC_CELLO  PCH_INTVRMEN 14												
GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>Bit 1</th><th>Bit 0</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI (default)</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	Bit 1	Bit 0	Boot Location	1	1	SPI (default)	1	0	PCI	0	0	LPC	+3.3V_RUN  GPIO51 12
Bit 1	Bit 0	Boot Location														
1	1	SPI (default)														
1	0	PCI														
0	0	LPC														
SATA1GP/GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	<table border="1"><tbody><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	1	0	PCI	0	0	LPC	 SATA1_GP						
1	0	PCI														
0	0	LPC														
			WEAK INTERNAL PULLUPS ON BOTH PIN. DEFAULT SPI BOOT DEVICE.													
SATA2GP/GPIO36	DMI RX Termination	PWROK	weak internal pull-down 0 = DMI RX is terminated to VSS. 1 = DMI RX is terminated to VCC/2.													
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = Disable ME Crypto TLS cipher suite. 1 = Enable Intel ME Crypto TLS cipher suite. Must be pulled up to support IntelR AMT with TLS and Intel SBA with TLS.	+3.3V_RUN  9424 change to NVPRO 11mm												
HDA_SDO	Flash Descriptor Security Override /ME Debug Mode	PWROK	weak Internal pull-down 0 = Normal Operation (Default) 1= Security Override	30 PCH_MELOCK  FDT_OVRD 14												
HDA_DOCK_EN#/GPIO33	DMI TX Termination	PWROK	internal pull-down. 0 = DMI TX is terminated to VSS. 1 = DMI TX is terminated to VCC/2.	 GPIO33 14												
GPIO62/ SUSCLK	PLL On-die PWR Voltage regulator Enable	RSMRST#	0 = Disable 1 = Enable (Default)	14 PCH_SUSCLK 												
GPIO8	Intel Reserved	RSMRST#	This signal must be pulled low when strap is sampled.	 GPIO8 14												
DDPB_CTRLDATA	Port B detection	PWROK	0 = Default, not detected 1 = Detected	+3.3V_RUN0  DDPB_CTRLDATA 15												
DDPC_CTRLDATA	Port C detection	PWROK	0 = Default, not detected 1 = Detected	+3.3V_RUN0  DDPC_CTRLDATA 15												
DDPD_CTRLDATA	Port D detection	PWROK	0 = Default, not detected 1 = Detected	+3.3V_RUN0  DDPD_CTRLDATA 15												
DSWVRMEN	Deep Sx well on the regulator enable	ALWAYS	0 = Disable 1 = Enable	+RTC_CELLO  PCH_DSWVRMEN 14												

## EMI



## SMBus/SMLink

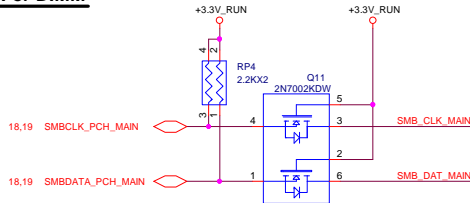


Close to PCH

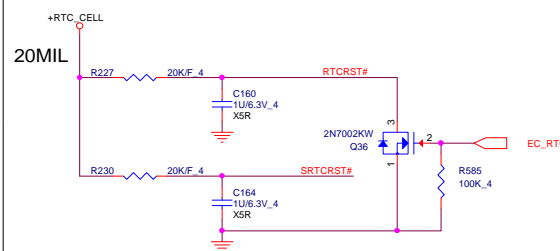
PCH PWROK



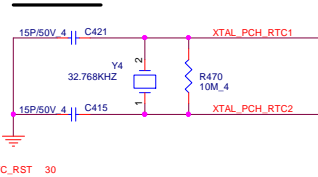
**For DIMM**



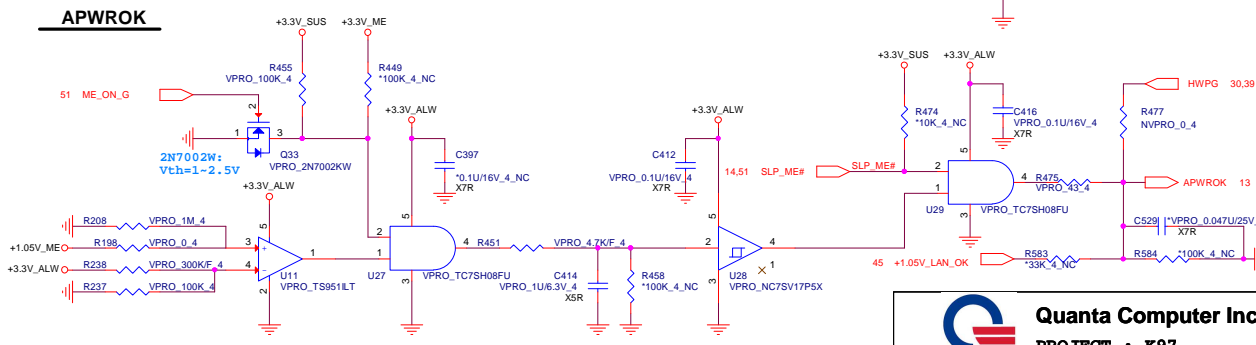
RTC



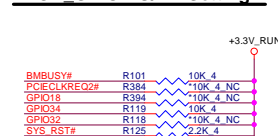
## XTAL



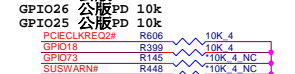
**APWROK**



## PCH\_GPIO PU/PD Setting



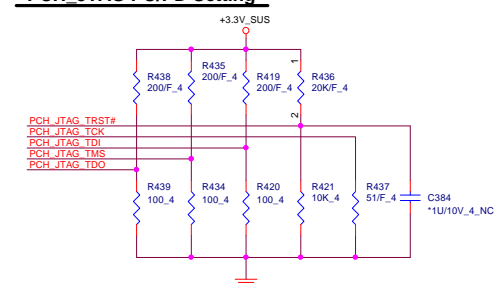
GPIO73 公版PD



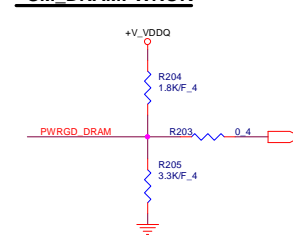
GPIO31 公版PD 10K NA



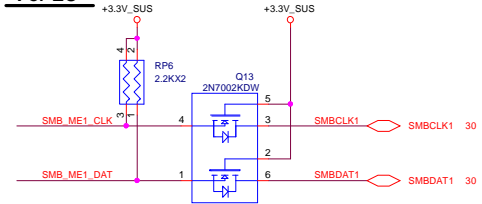
## PCH JTAG PU/PD Setting



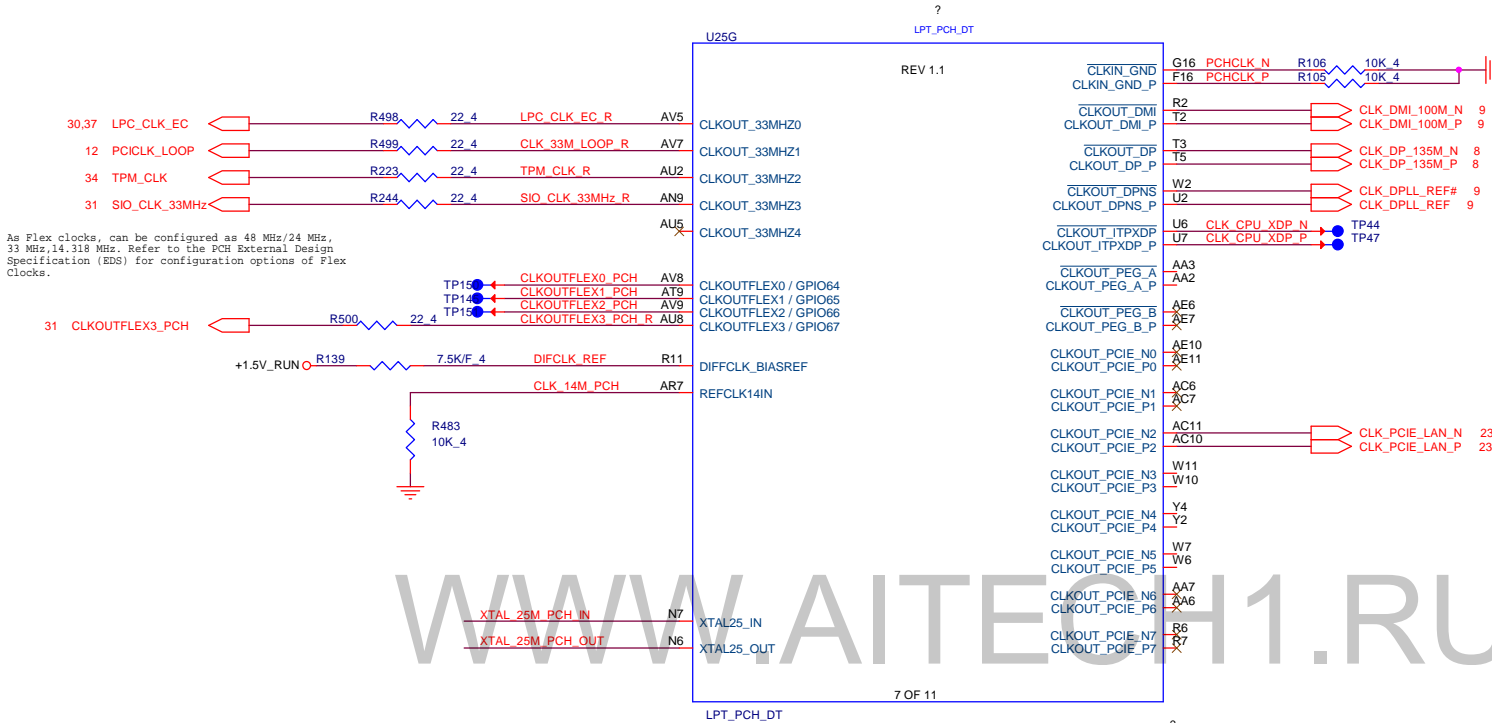
## SM DRAMPWROK



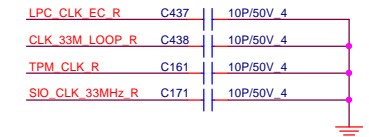
**For EC**



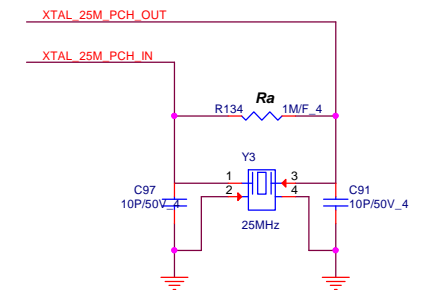




## EMI



## PCH XTAL



DESIGN NOTE:  
STUFF ALWAYS

DESIGN NOTE:  
Ra DAMPING RESISTOR DO NOT CHANGE TO 0402.

## VGA Disable

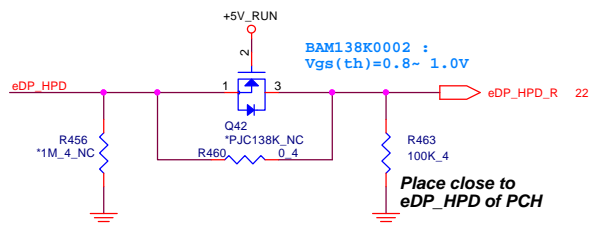
PDG r2\_1\_1 PG157

## VGA DAC Disable Recommendations

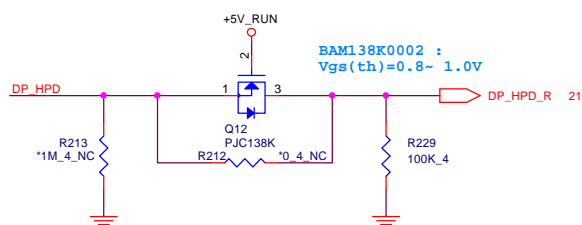
Signal Name	Recommended Connection
VGA_RED, VGA_GREEN, VGA_BLUE	NC or GND
VGA_IRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_IREF	GND
DDC_CLK, DDC_DATA	NC
VCCADAC	GND
VCCADACBG	GND

Note :  
Straps for digital ports B, C and D.  
For DisplayPort\* - Should be pulled to 3.3V through a 2.2K ohms resistor to configure digital port.  
PS: reference page13 straps

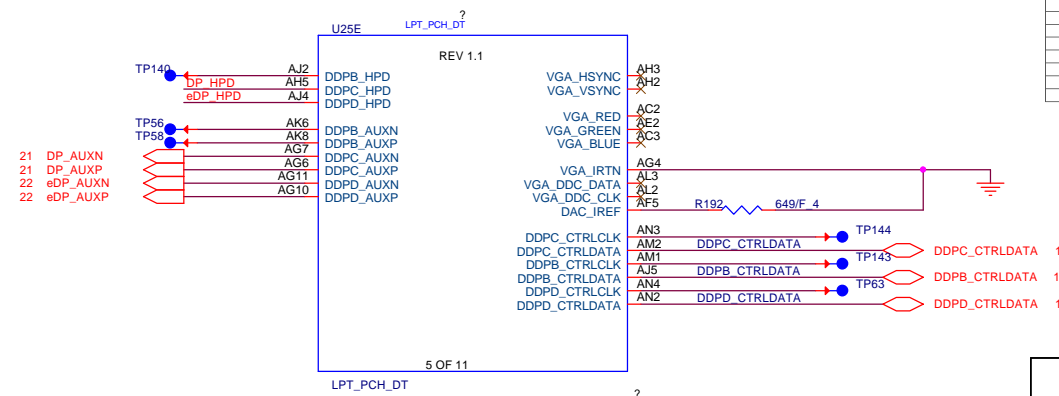
## eDP HPD

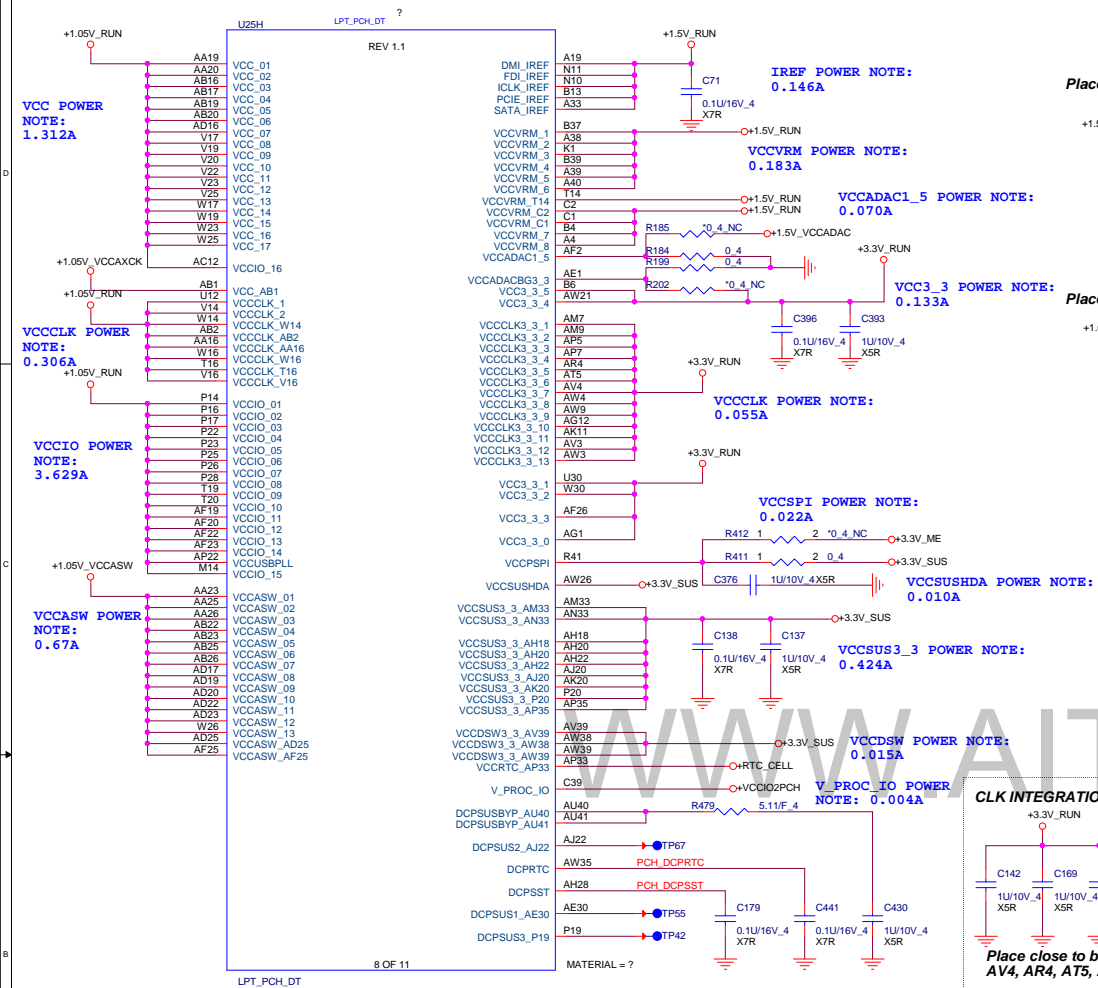


## DP HPD

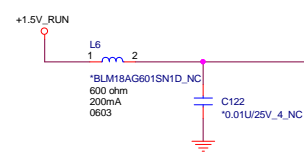


Note : AIO PDG\_R2\_1\_1, PG108  
Select the pass-gate FET which has VGSTH less than 1.5 V.



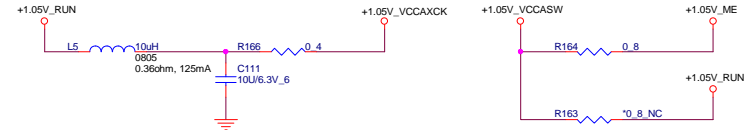


**Place within 100mils from PCH**

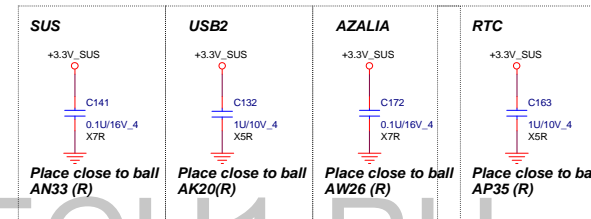


POWER NOTE:  
0.07A

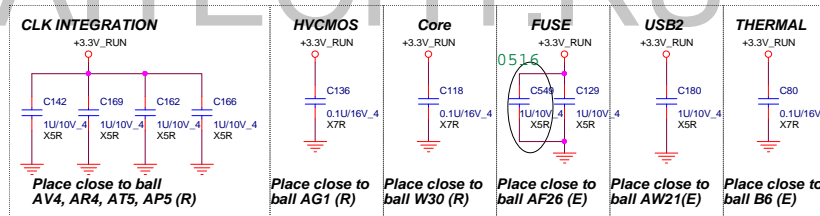
**Place within 100mils from PCH**



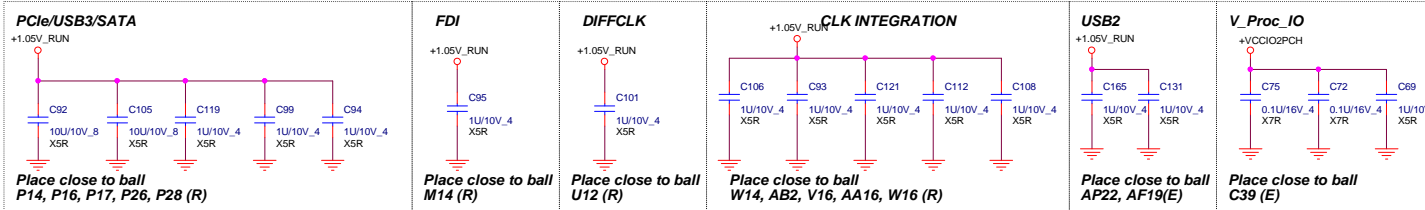
**V3.3 S5**



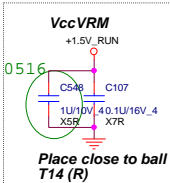
## V3.3 S0



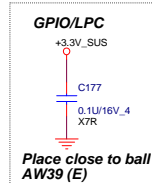
**V1.05S**



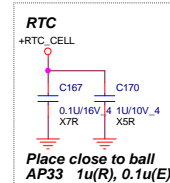
## V1.5 S0



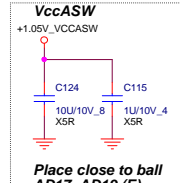
**V3.3A**



## V3.3RTC

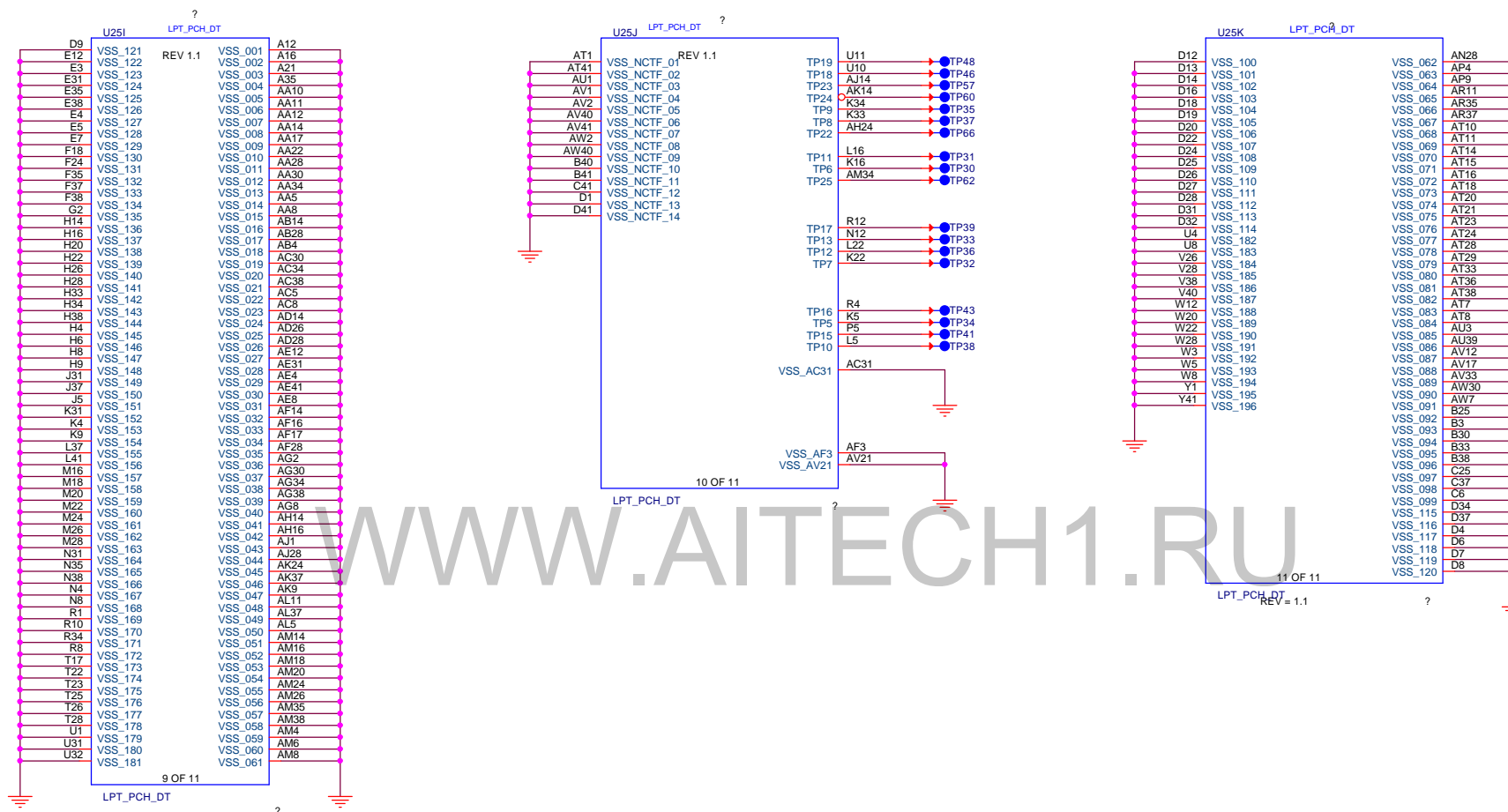


**V1.05M**



NOTE: PDG\_r2\_1\_1 PG472  
Placement type:  
(R)unway, (E)dge, (B)Back

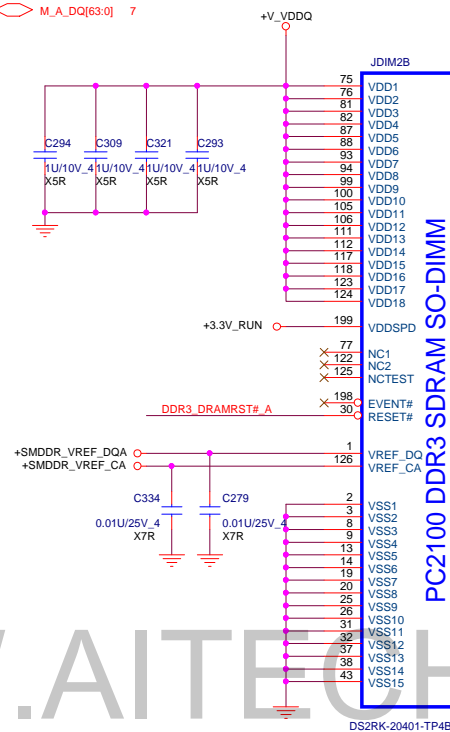
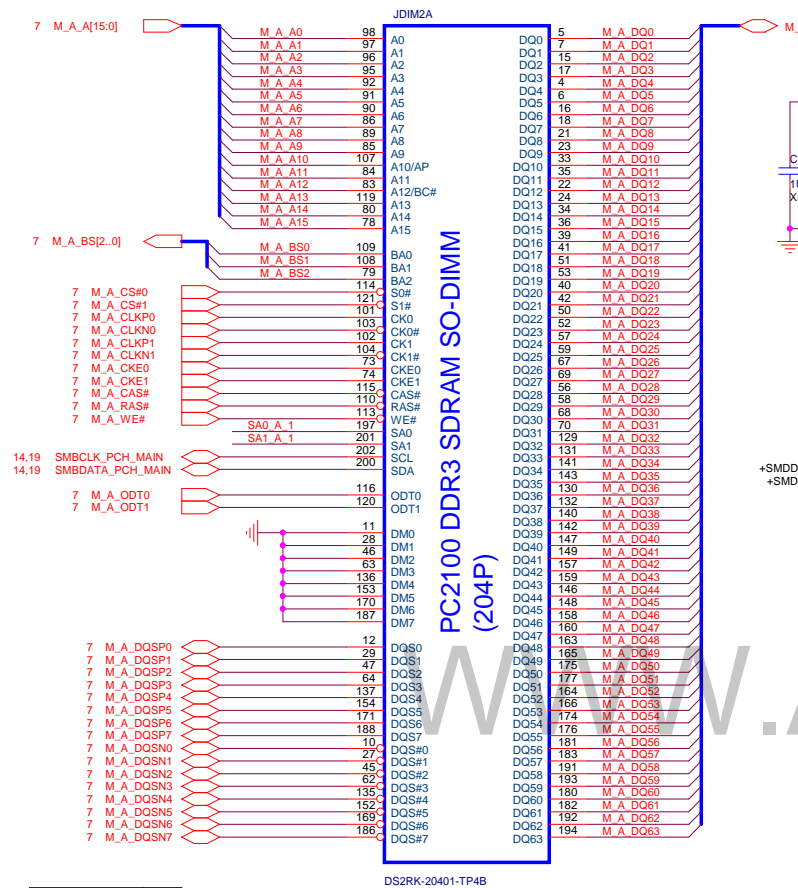




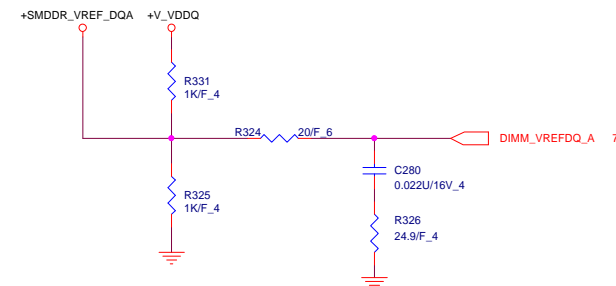
Quanta Computer Inc.

PROJECT : K97

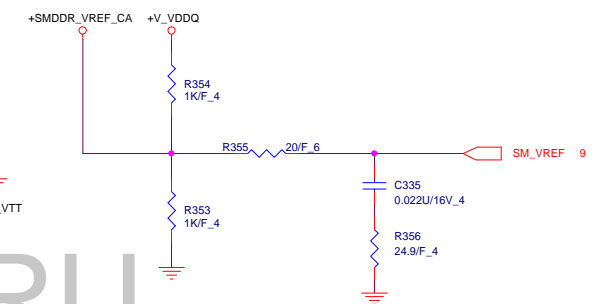
Size	Document Number	Rev
	PCH_GND	1A
Date:	Thursday, June 12, 2014	Sheet 17 of 51



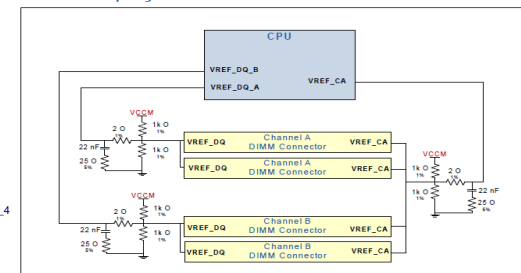
## Memory VREF\_DQ\_A



## Memory VREF\_CA

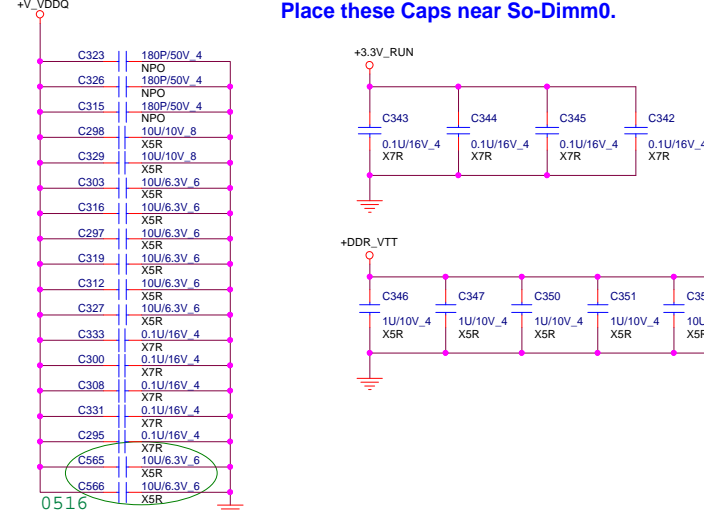


## DDR3 VREF Topologies



On "Bottom side"

Place these Caps near So-Dimm0.

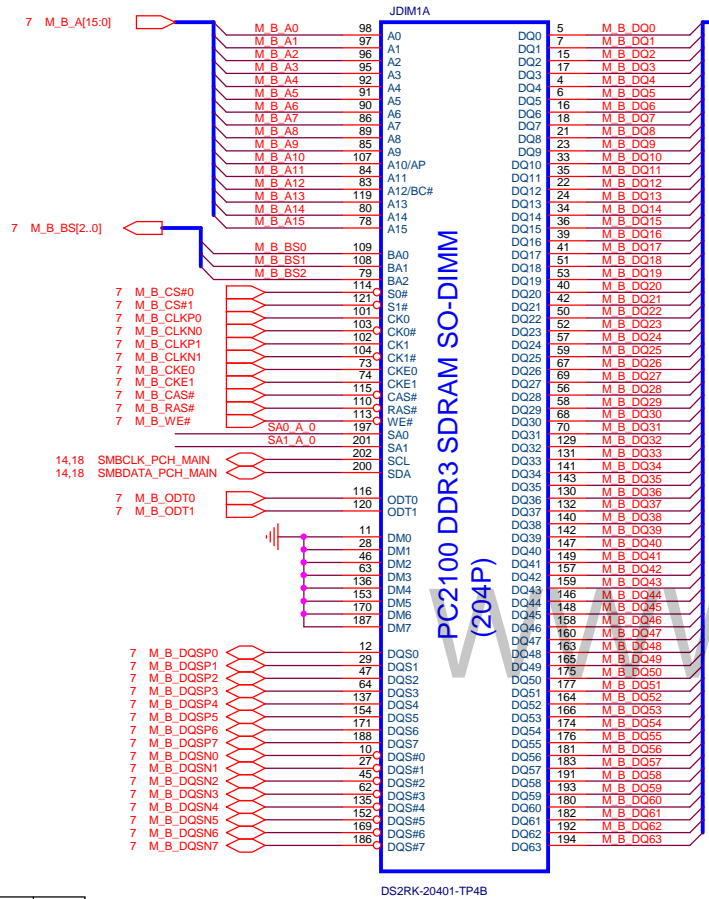


Quanta Computer Inc.

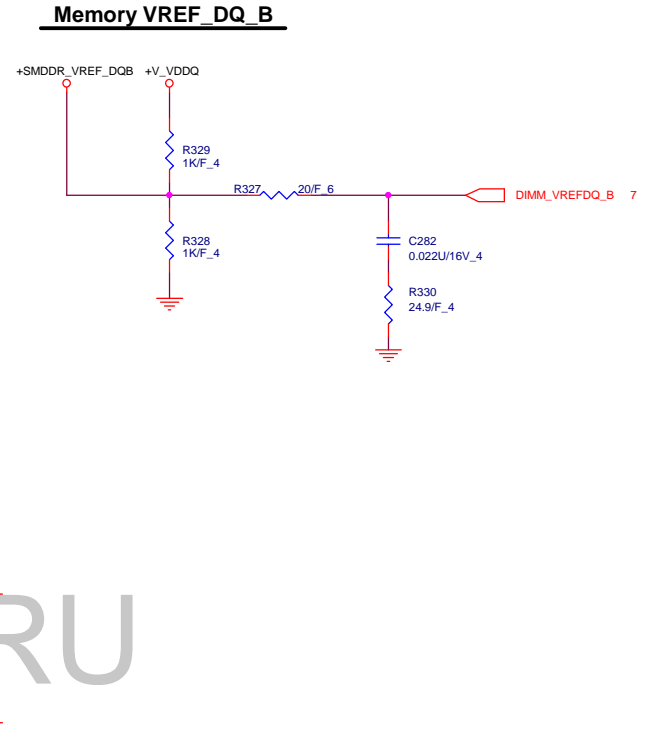
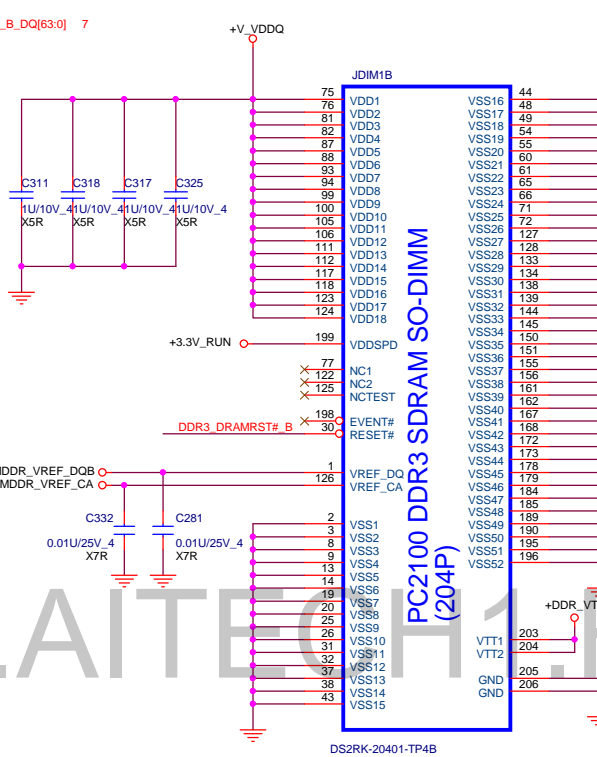
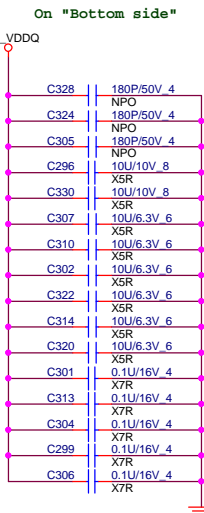
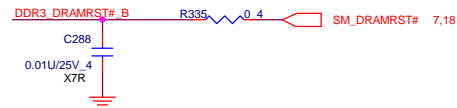
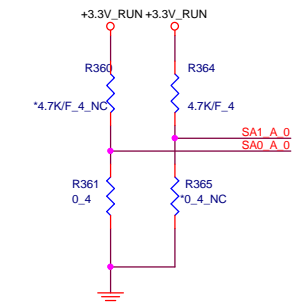
PROJECT : K97

Size	Document Number	Rev
	DDR3 CHA DIMM 0	A
Date:	Thursday, June 12, 2014	Sheet 18 of 51

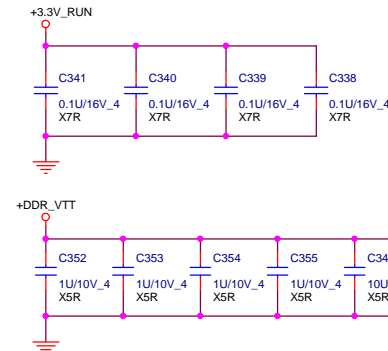
CHANNEL B DIMM 0 (H=4, RVS)



SPD SA0	0
SPD SA1	1



**Place these Caps near So-Dimm0.**



0516



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PROJECT : K97

Size	Document Number <b>DDR3 CHB DIMM 0</b>	Rev <b>A</b>
Date:	Thursday, June 12, 2014	Sheet 19 of 51

# USB2.0 HUB for MB

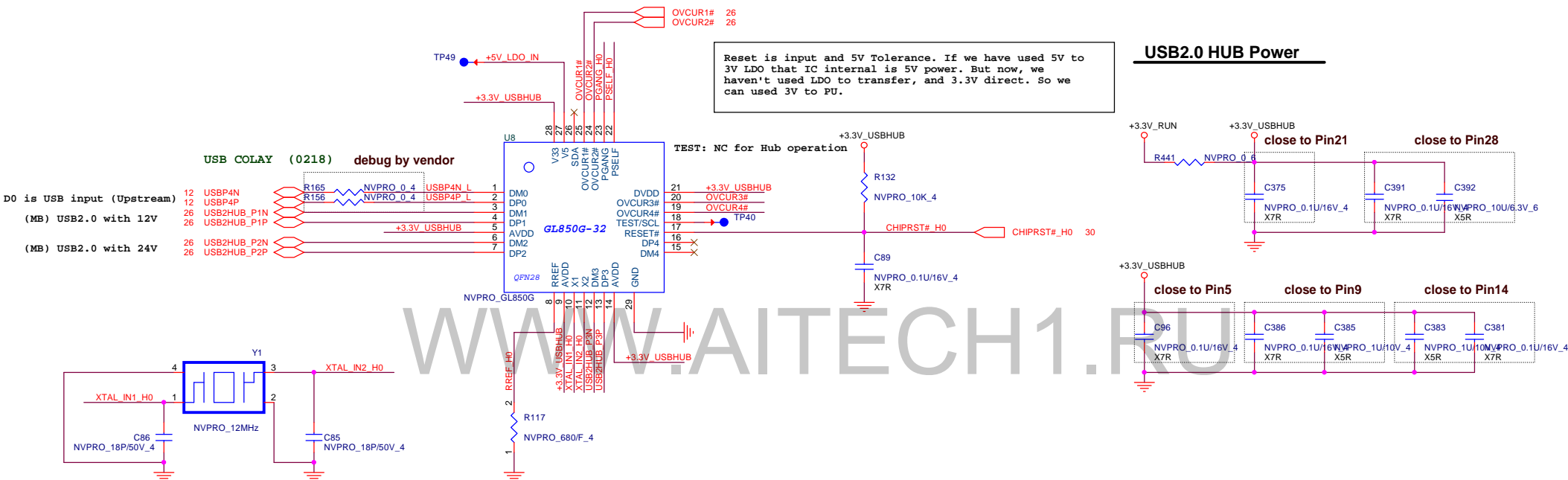
## USB HUB COLAY

Q87	All of NC
H81	All of POP

+5V\_LDO\_IN:  
This is 5V input if we use internal  
LDO to transfer 5V to 3V3.  
This Pin can be reserve to floating

Reset is input and 5V Tolerance. If we have used 5V to 3V LDO that IC internal is 5V power. But now, we haven't used LDO to transfer, and 3.3V direct. So we can used 3V to PU.

## USB2.0 HUB Power

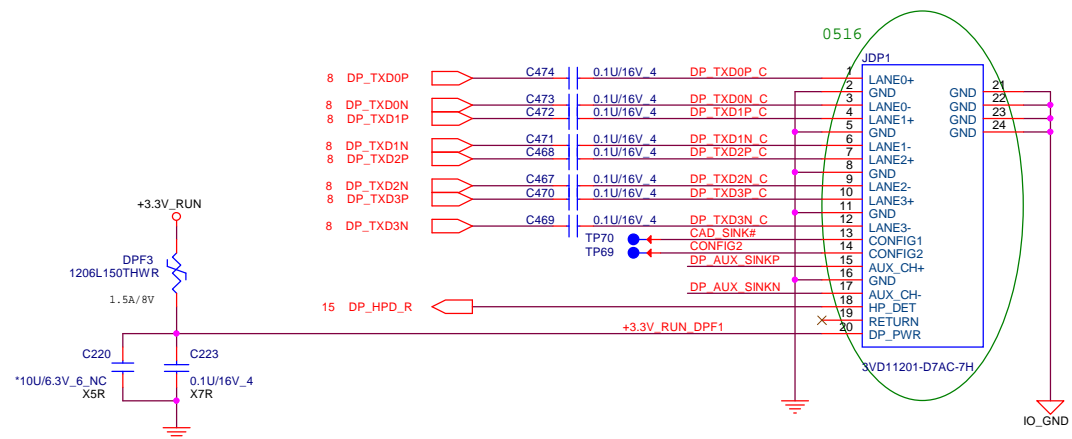


## [Strapping]

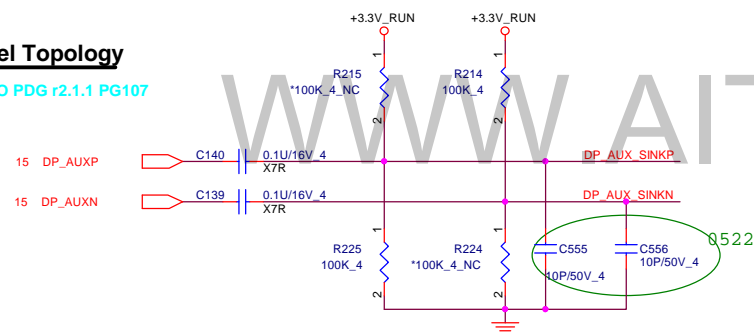
PGANG	PSELF	OVCURn#	Port Disable setting	TEST
H Gang mode: when OC occur, turn off all USB port	H Power Self: For 500mA device	Floating For Non-removable device	Port Number Pull Port	0 NC: Normal hub operation
L Individual mode: When OC occur, turn off OC port	L Power Bus: For 100mA device max	Pull high For Removable device	1 (Port1) Port 2 Pull High	1 Chip will be put in test mode
			2 (Port 1/ 2) Port 3 Pull High	
			3 (Port 1/ 2/ 3) Port 4 Pull High	



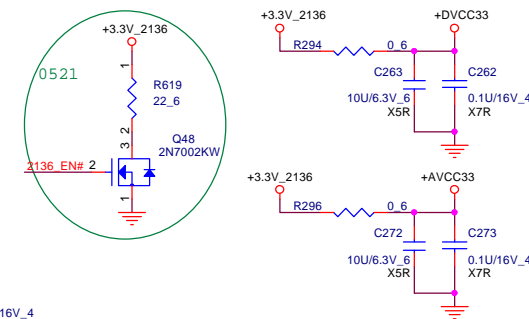
**Quanta Computer Inc.**  
**PROJECT : K97**

**DisplayPort****EMC****AUX Channel Topology**

AIO PDG r2.1.1 PG107

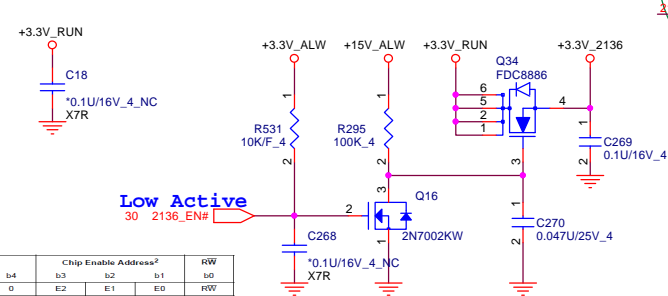
**Quanta Computer Inc.****PROJECT : K97**

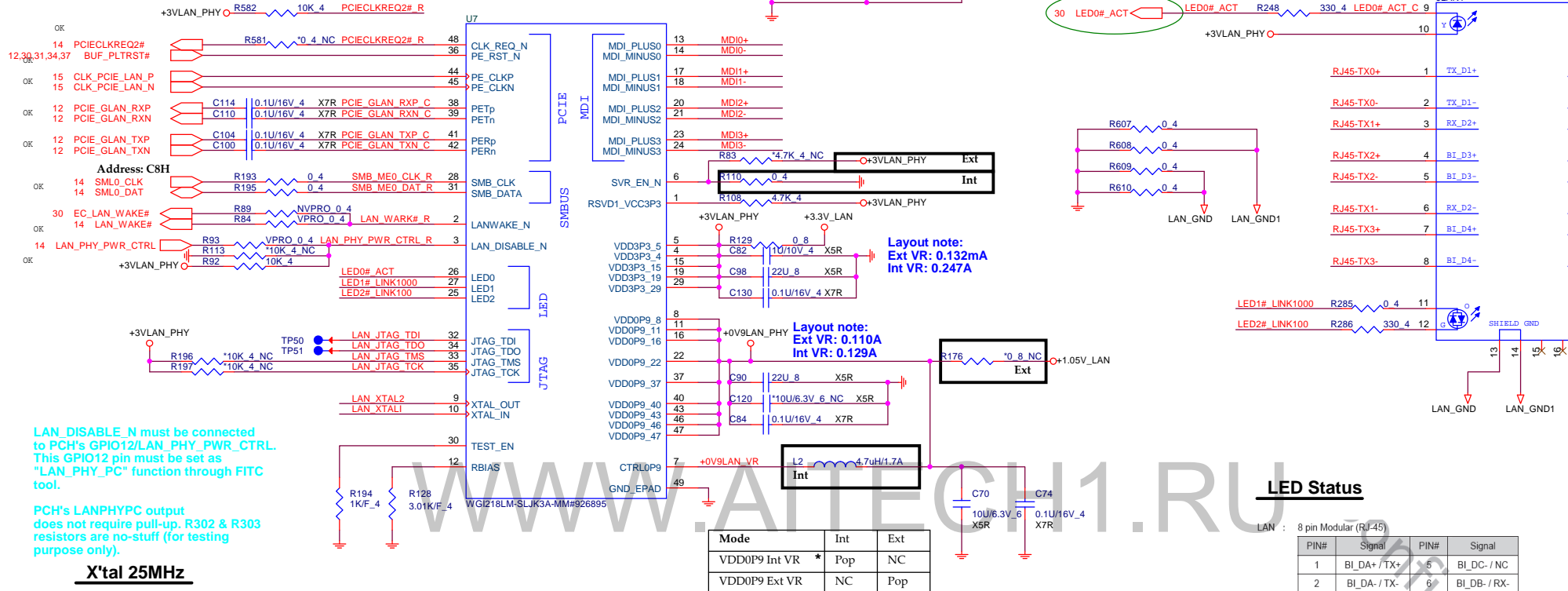
Size	Document Number	Rev
	<b>Display Port</b>	<b>A</b>
Date:	Thursday, June 12, 2014	Sheet 21 of 51



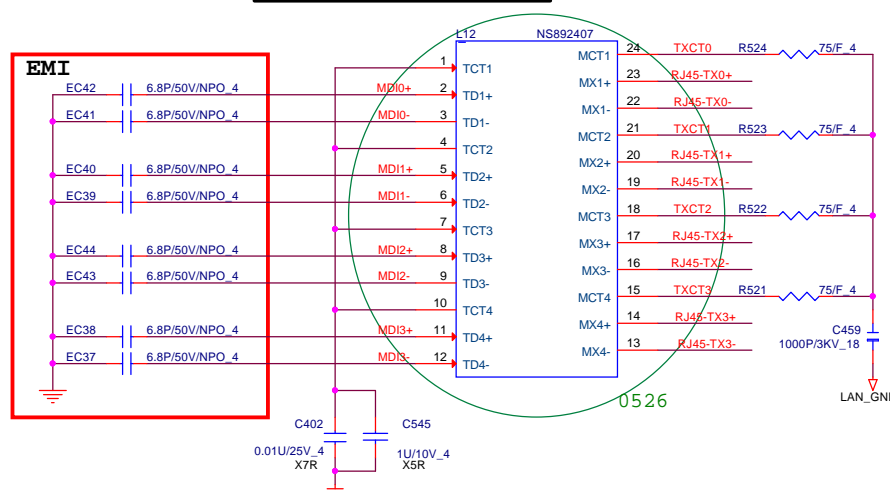
	Device Type Identifier <sup>1</sup>				Chip Enable Address <sup>2</sup>			R $\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	R $\overline{W}$

Note: 1. The most significant bit, b7, is sent first.  
 2. E0, E1 and E2 are compared against the respective external pins on the memory device.

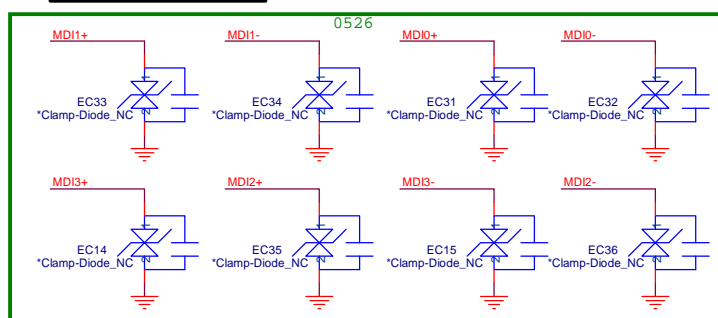




## 10/100/1000 Transformer



## EMI Suppression



## LAN Connector LED Status

LED	LED Color	LED Status	Condition
Link	Green	Off	LAN link is not established.
Activity	Yellow	On	LAN link is established.
Speed	Green	Blinking	LAN activity is occurring.
	Green	Off	10 Mbps data rate
	Green	On	100 Mbps data rate
	Yellow	On	1 Gbps data rate

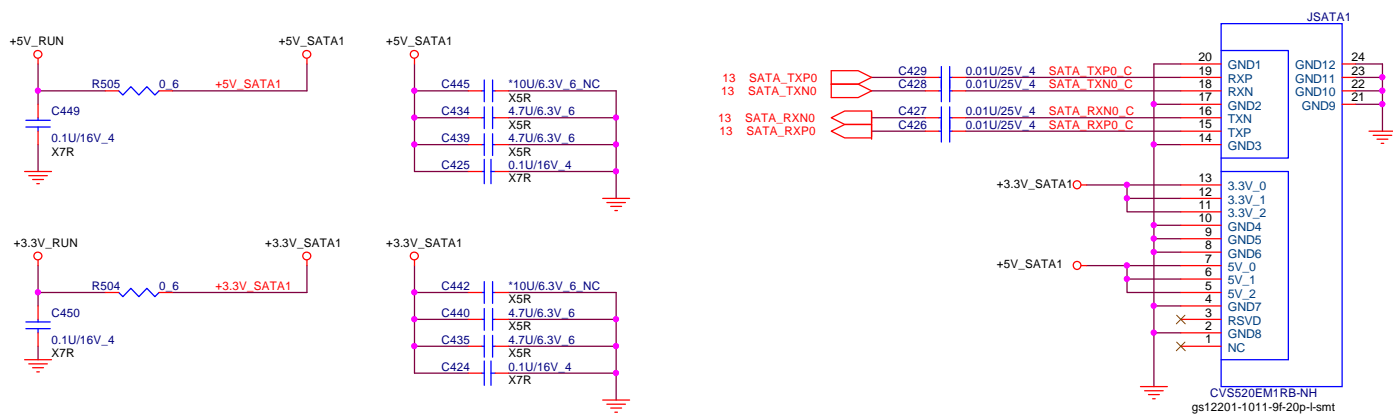
## LED Default Values

LED	Mode	Color	Blink	Polarity
LED0	Link Up/Activity	Green	200 ms on/200 ms off	Active low
LED1	Link 1000	Yellow	No	Active low
LED2	Link 100	Green	No	Active low

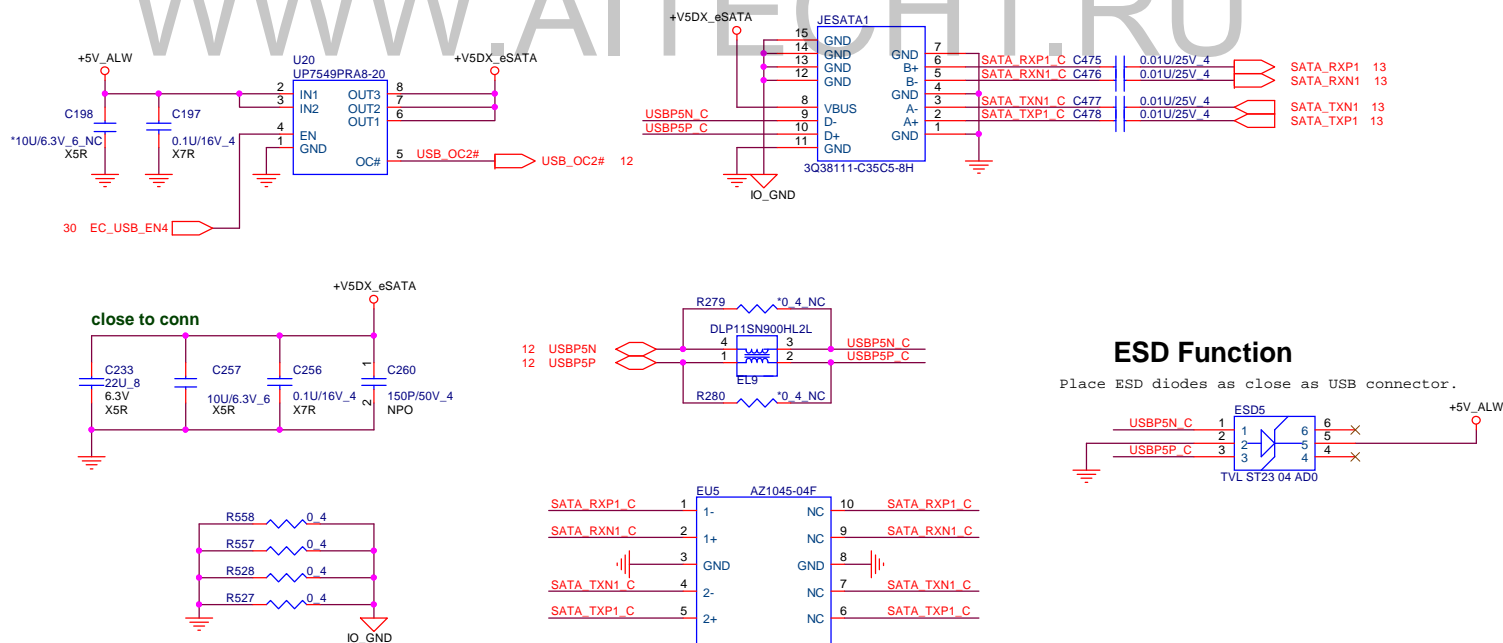


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### Internal SATA HDD Conn.



### eSATA Conn.



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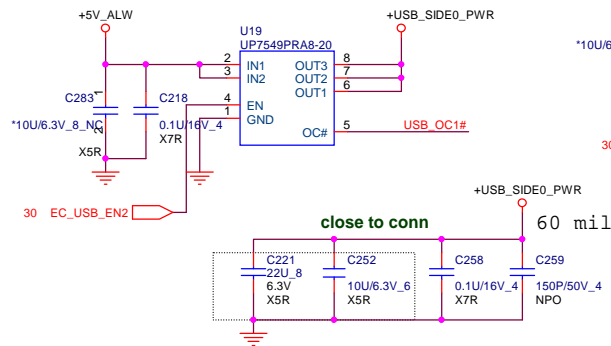
**PROJECT : K97**

Size	Document Number	Rev
	<b>SATA HDD/E-SATA WITH USB2</b>	<b>1A</b>
Date:	Thursday, June 12, 2014	Sheet 24 of 51

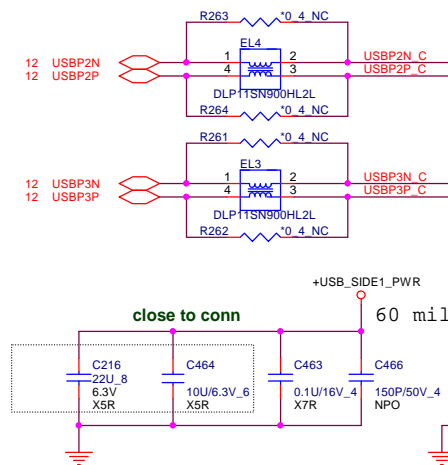
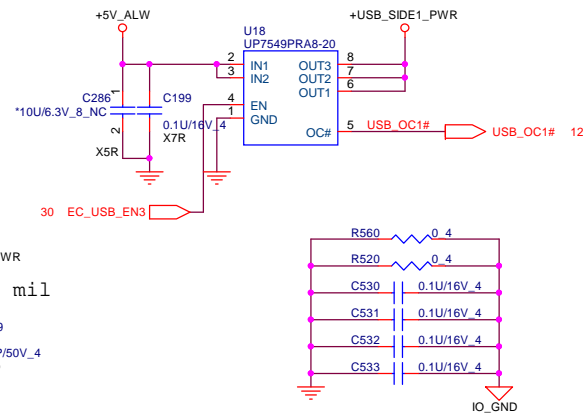


# USB2.0\*2

## USB2.0 OC for Port0

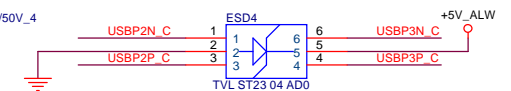


## USB2.0 OC for Port1

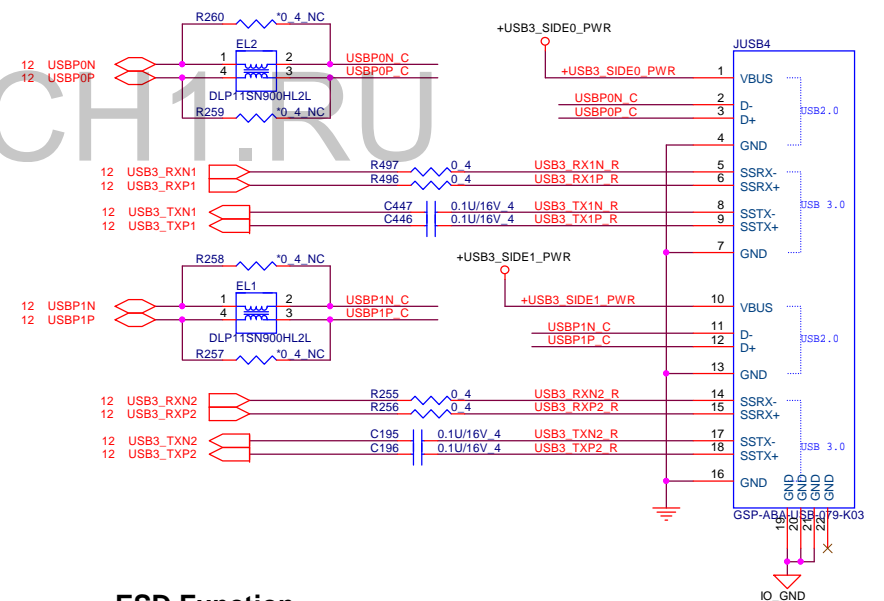
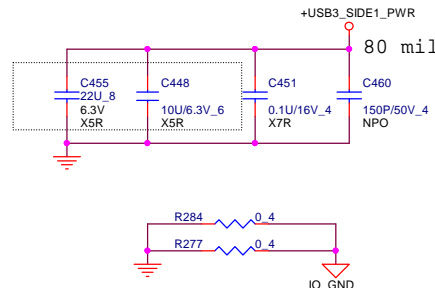
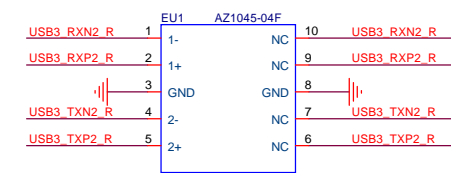
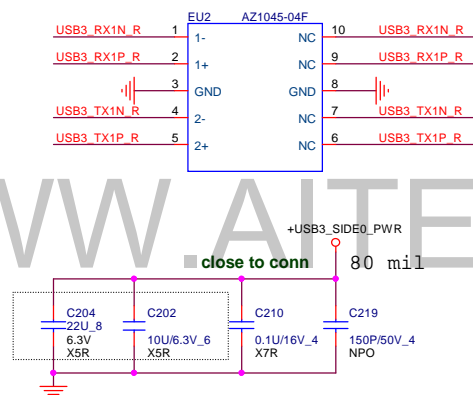
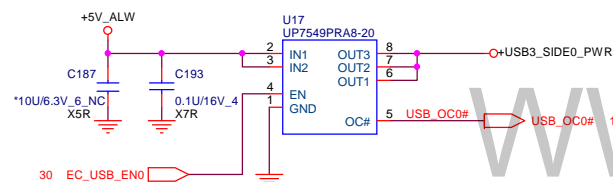


## ESD Function

Place ESD diodes as close as USB connector.

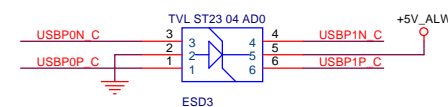


# USB3.0\*2



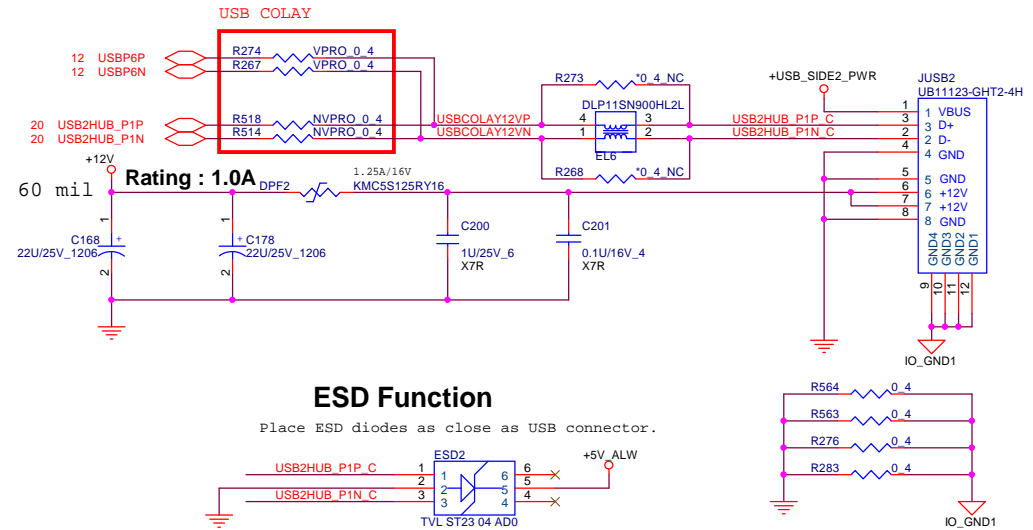
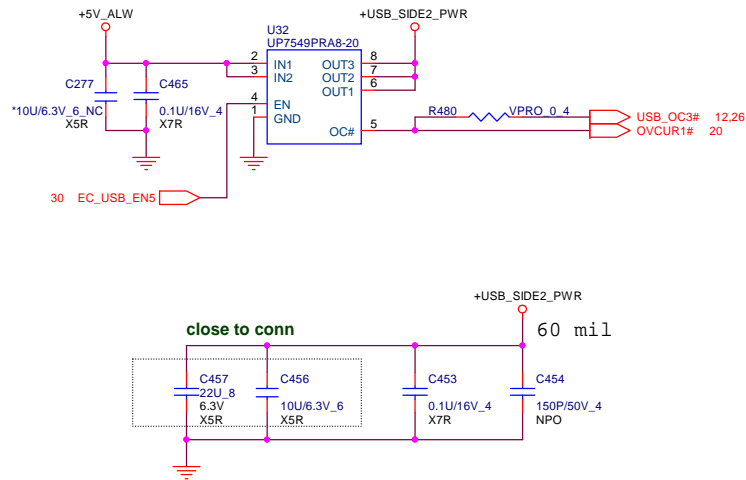
## ESD Function

Place ESD diodes as close as USB connector.



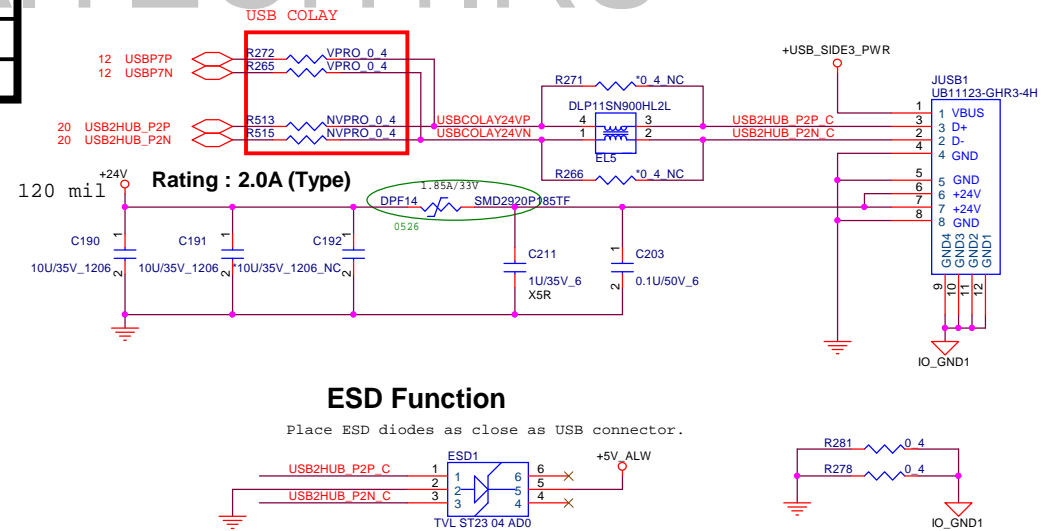
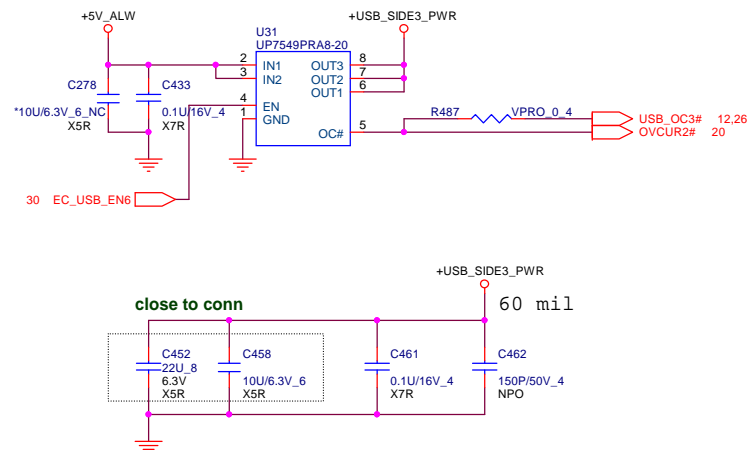
Size	Document Number	Rev
	USB2*2/USB3*2	A
Date	Thursday, June 12, 2014	Sheet 25 of 51

# USB2.0 with 12V

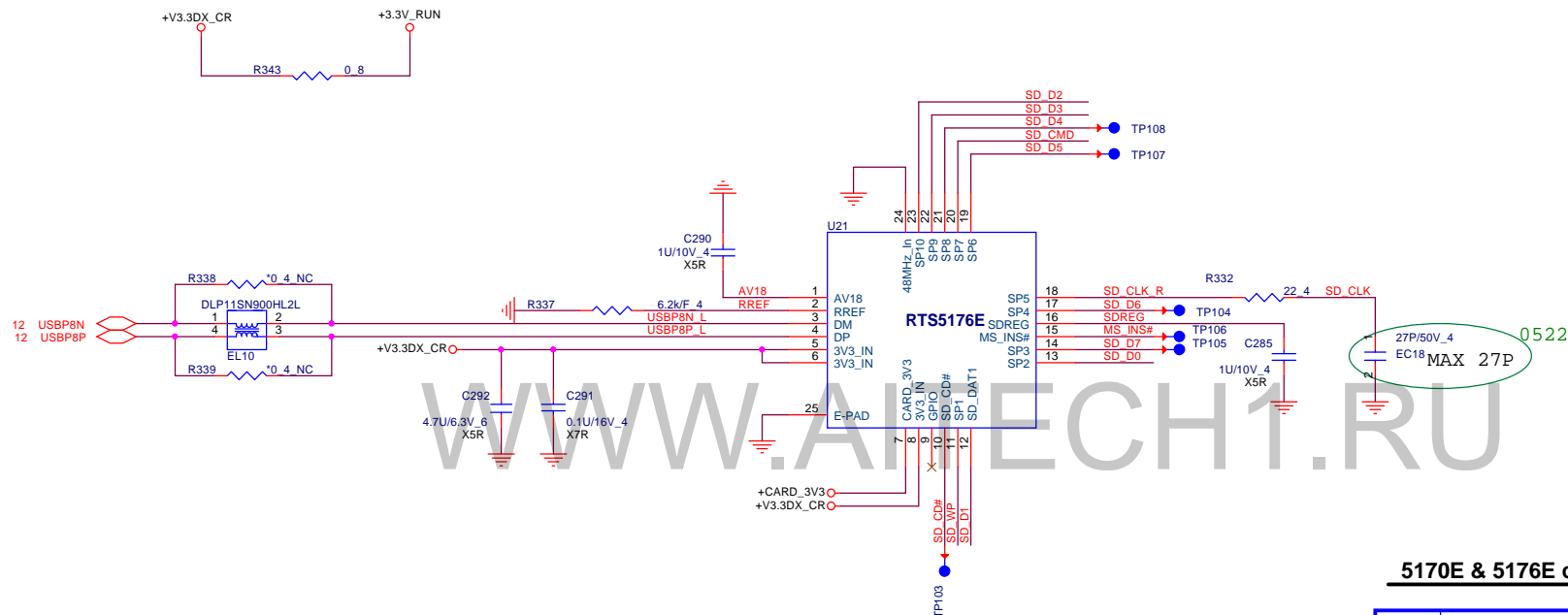


# USB2.0 with 24V

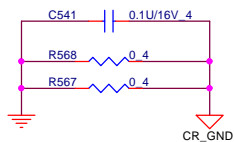
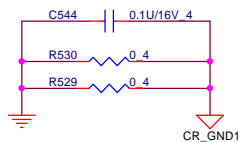
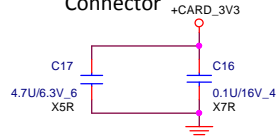
PCH	R518/R514/ R513/R515	R274/R267/ R272/R265/ R480/R487/
Q87	NC	POP
H81	POP	NC



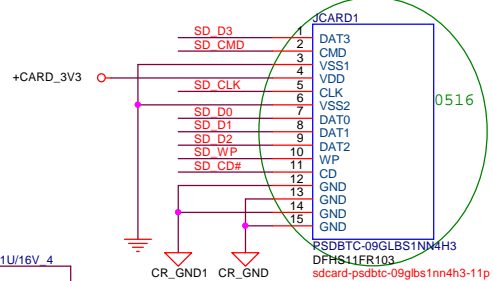
## Card Reader



Place close to  
Connector



## CARD READER



## 5170E & 5176E compare

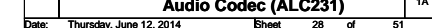
NAME	RTS5170E	RTS5176E
SP1	SD_WP & MC_CLK	SD_WP & MS_DAT1
SP2	MS_INS#	SD/MMC_DAT0 & MS_DAT5
SP3	SD_DAT1	MMC_DAT7 & MS_DAT4
SP4	SD_DAT0 & MS_DAT7	MMC_DAT6 & MS_DAT0
SP5	SD_DAT7 & MS_DAT3	SD_CLK & MS_DAT2
SP6	SD_CD#	MMC_DAT5 & MS_DAT6
SP7	SD_DAT6 & MS_DAT6	SD/MMC_CMD & MS_DAT3
SP8	SD_CLK & MS_DAT2	MMC_DAT4 & MS_DAT7
SP9	SD_DAT5 & MS_DAT0	SD/MMC_DAT3 & MS_CLK
SP10	SD_CMD	SD/MMC_DAT2 & MS_BS
SP11	SD_DAT4 & MS_DAT5	
SP12	SD_DAT3 & MS_DAT1	
SP13	SD_DAT2 & MS_DAT4	

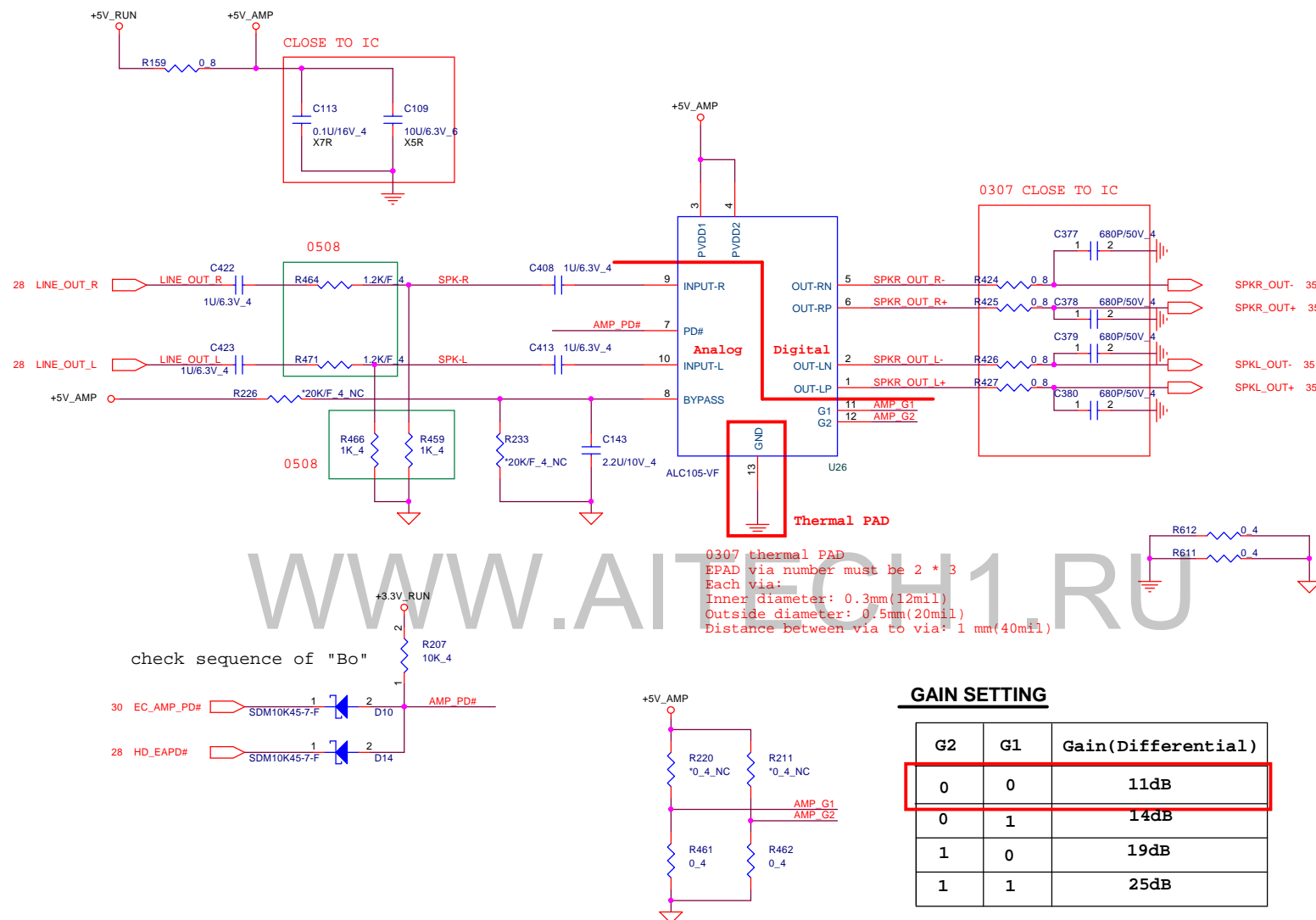


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**Card Reader (RTS5176E)**





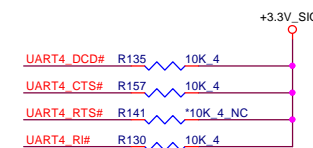
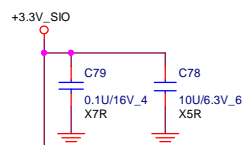
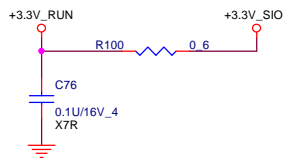
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**PROJECT : K97**

**STEREO\_AMP**

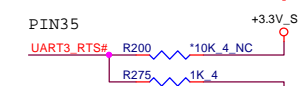
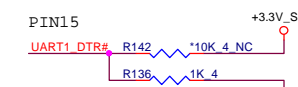
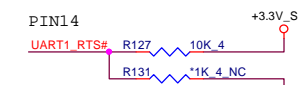


## Standby Power



## Strapping Setting

PIN	Name	0	1
14	2E_4E_SEL	2E	4E
15	24_48_SEL	24M CLK	48M CLK
35	SOUTC_P80_SEL	Disable	Enable



Note:  
Most pul-ups are provided on system main-board.

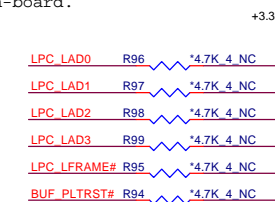


Table 41-4. Firmware Hub Interface Signals

Name	Type	Recommendations	Reason/Impact
FWH[1:0] / LAD[3:0]	I/O	No external pull-ups required. Connect straight to FWH/LPC	PCH Integrates 20 kΩ nominal pull-up resistors on these signal lines.
FWH[4] / LFRAME#, LDRQ[0], LDRQ[1], LDRQ[2]	O	No external pull-ups required. Connect straight to FWH/LPC	PCH Integrates 20 kΩ nominal pull-up resistors on these signal lines.

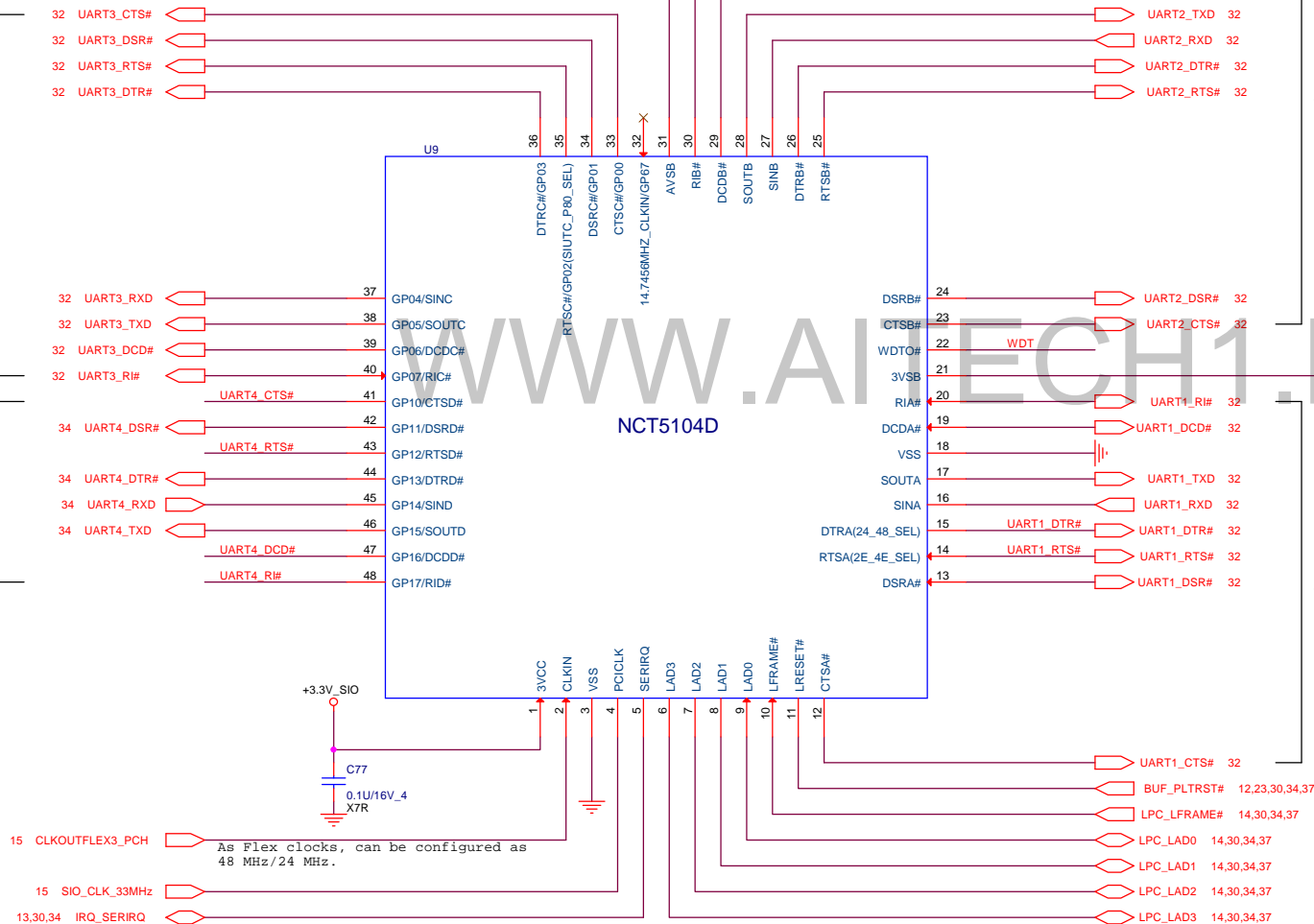
UART3

VFD

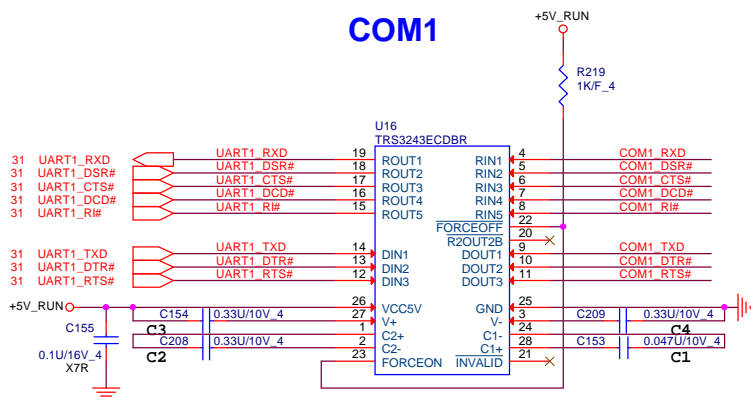
UART2

UART1

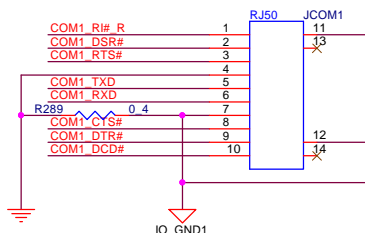
NCT5104D



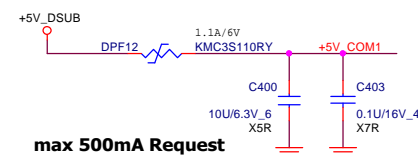
## COM1



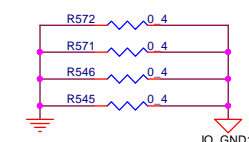
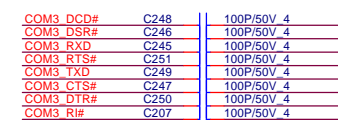
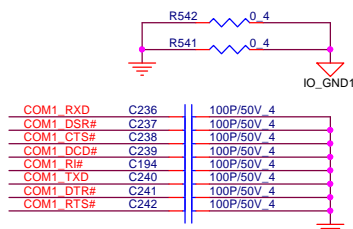
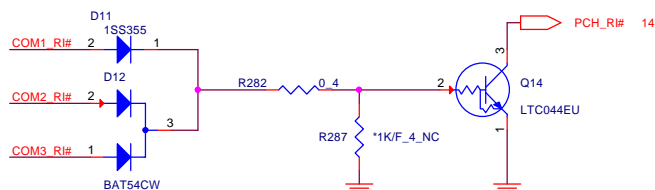
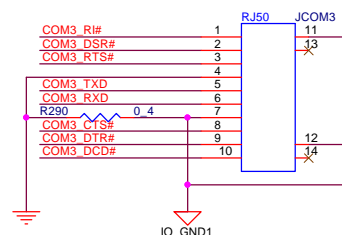
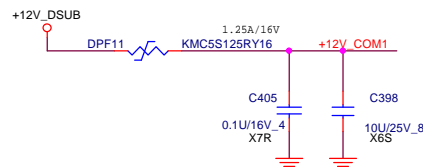
RJ type 10 pin (TBD 1)					
PIN#	Signal	PIN#	Signal	PIN#	Signal
1	R1 (default) / +5 V / +12 V (1)	6	RXD		
2	DSR	7	SG/FG		
3	RTS	8	CTS		
4	GND	9	DTR		
5	TXD	10	DCD		



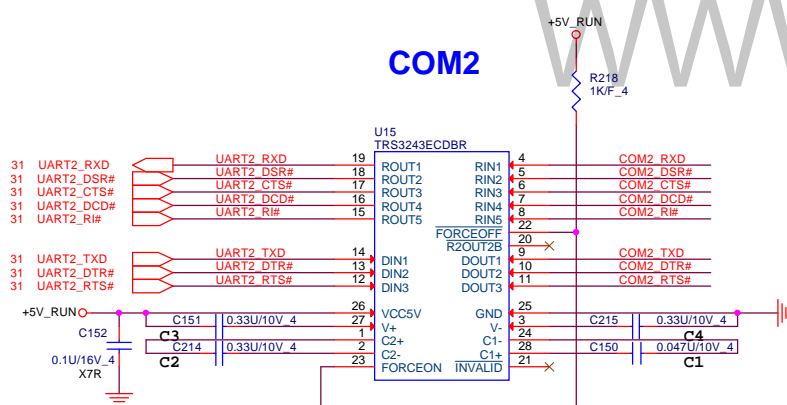
## max 500mA Request



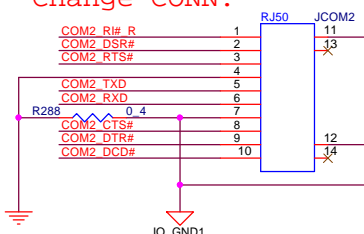
## max 500mA Request



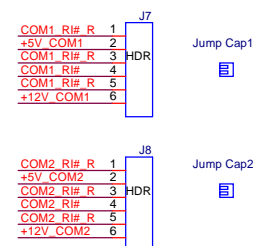
## COM2



## Change CONN.



## COM1/COM2 JUMP SWITCH



## TRS3243E SPEC

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF



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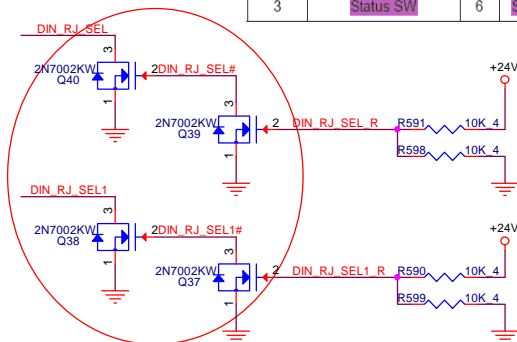
For RJ Drawer

PIN#	Signal	PIN#	Signal
1	GND	4	CD Drive (+24V)
2	CD return (GND)	5	RJ/DIN
3	Status SW	6	Status SW return

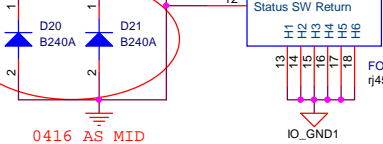
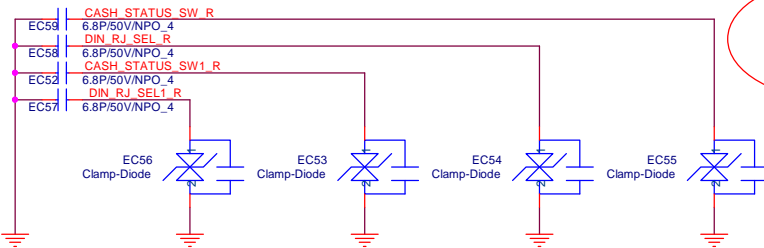
For DIN Drawer

PIN#	Signal	PIN#	Signal
1	GND	4	CD Drive (+12V)
2	CD return (GND)	5	RJ/DIN
3	Status SW	6	Status SW return

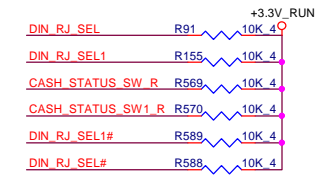
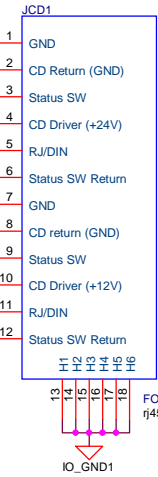
## Cash drawer



0425 change to BAM70020041

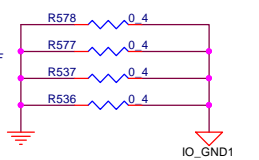


RJ11

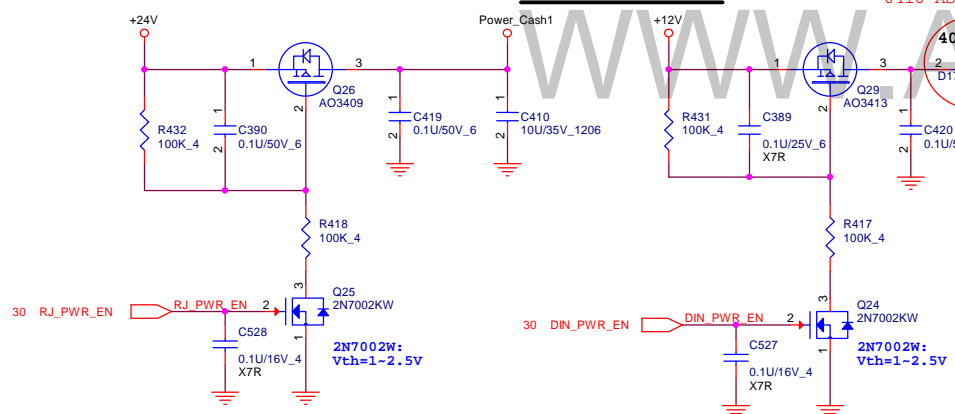


TYPE1 1A(12V)

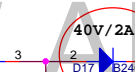
TYPE2 1.16A(24V)



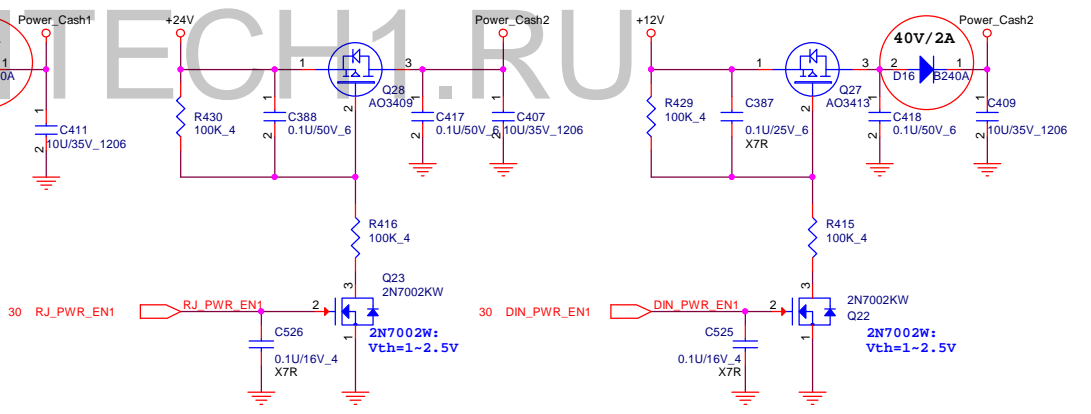
### RJ & DIN detect1



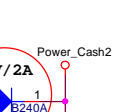
0416 AS MID



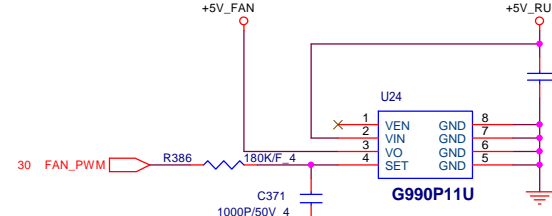
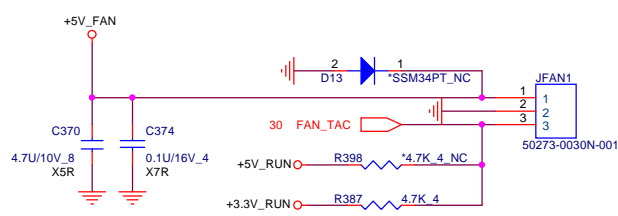
### RJ & DIN detect2



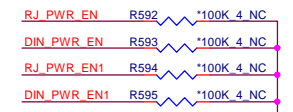
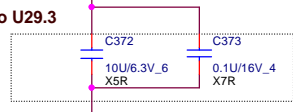
0416 AS MID



### FAN

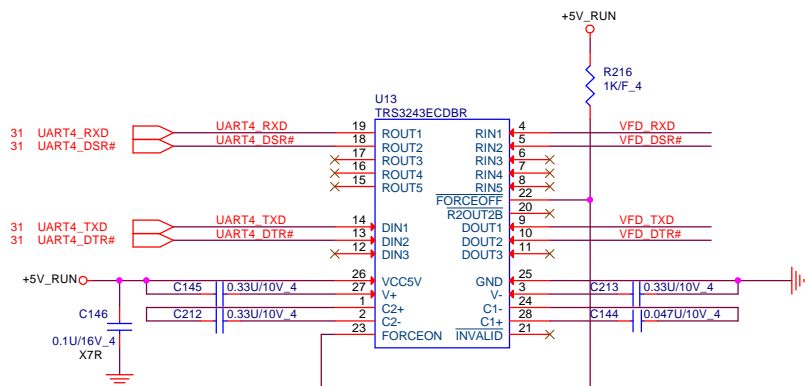


close to U29.3



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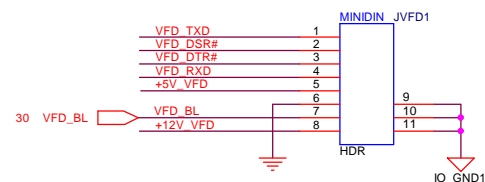
## VFD



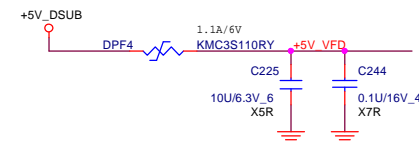
VFD (Serial port COM4 for Rear Display):

8 pin Mini-Din

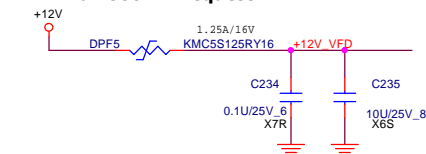
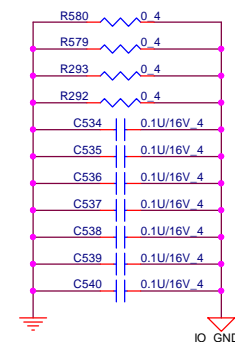
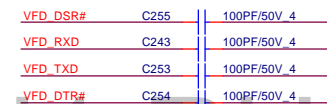
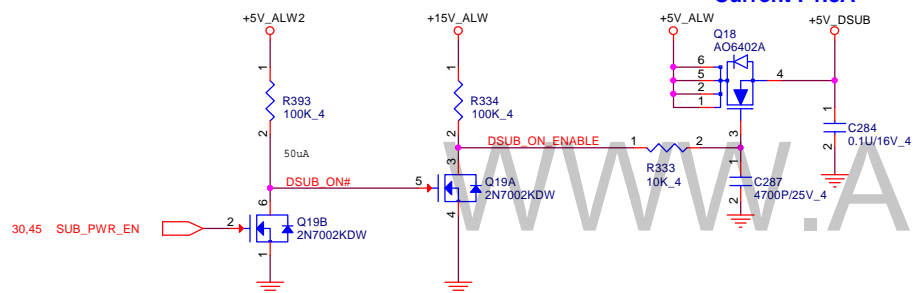
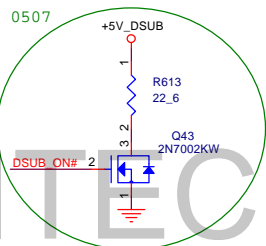
PIN#	Signal	IN/OUT	PIN#	Signal	IN/OUT
1	TXD	OUT	5	+5 V	Power
2	DSR	IN	6	GND	GND
3	DTR	OUT	7	2 <sup>nd</sup> LCD backlight ON/OFF	OUT
4	RXD	IN	8	+12 V	Power



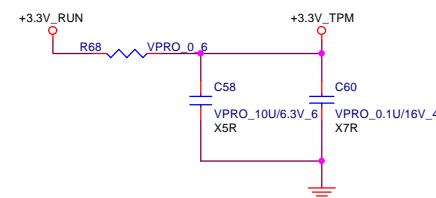
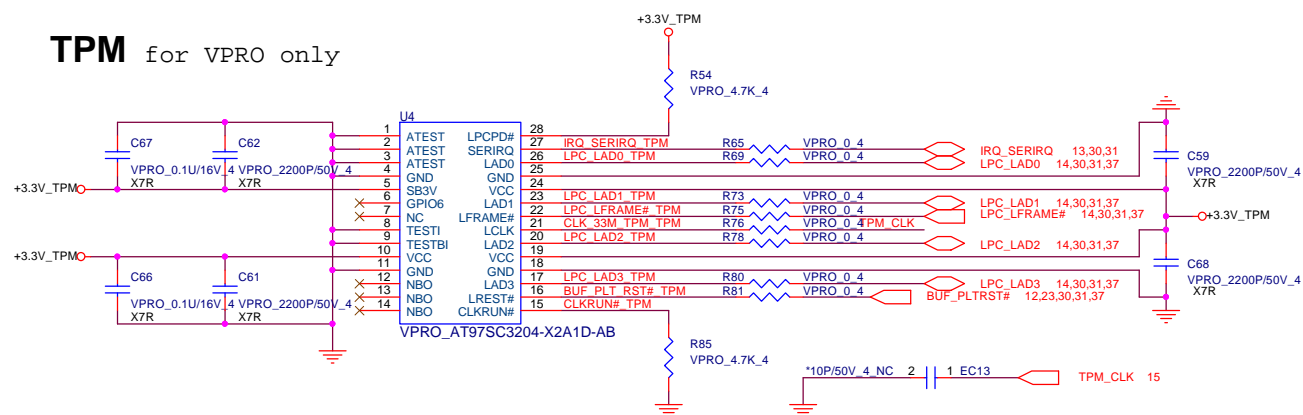
max 800mA Request



max 800mA Request

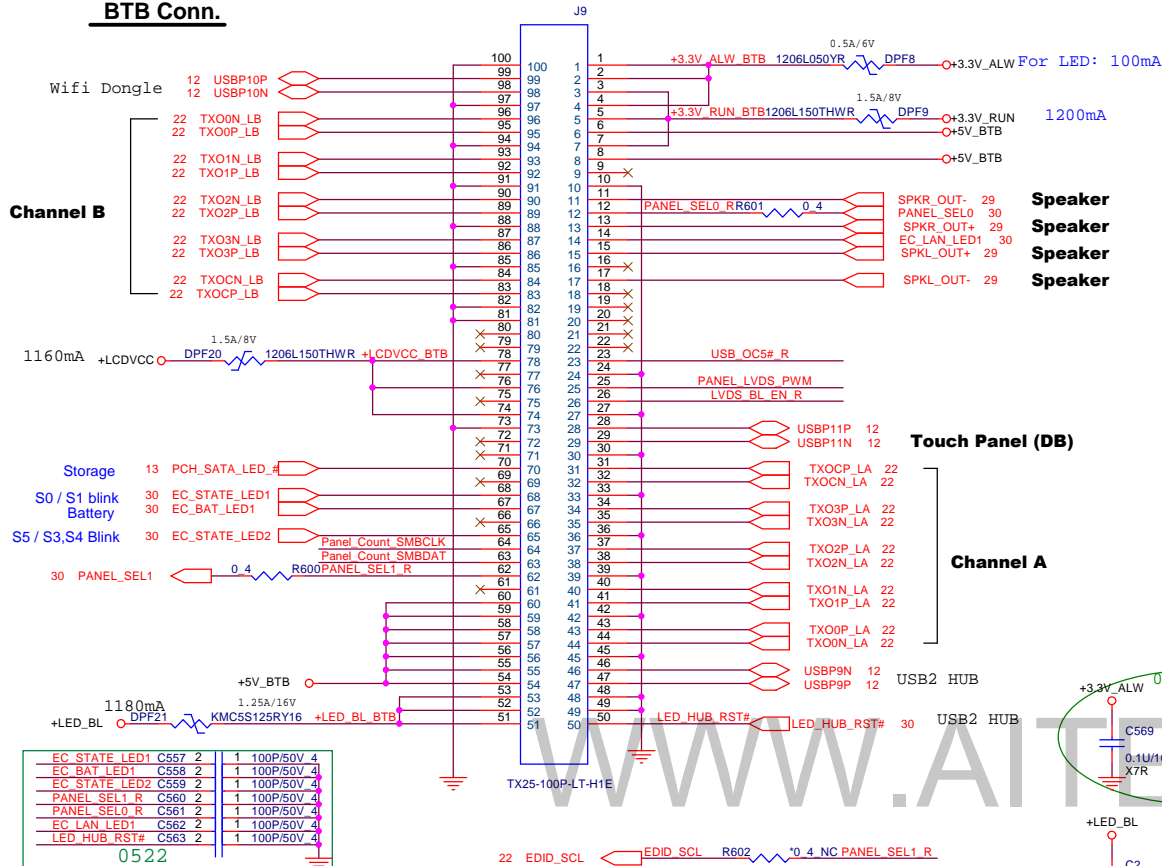
+5V\_DSUB  
Current : 1.8A

## TPM for VPRO only

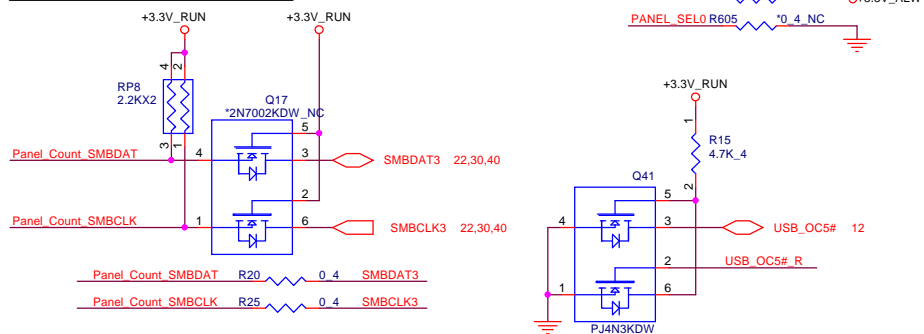


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## BTB Conn.



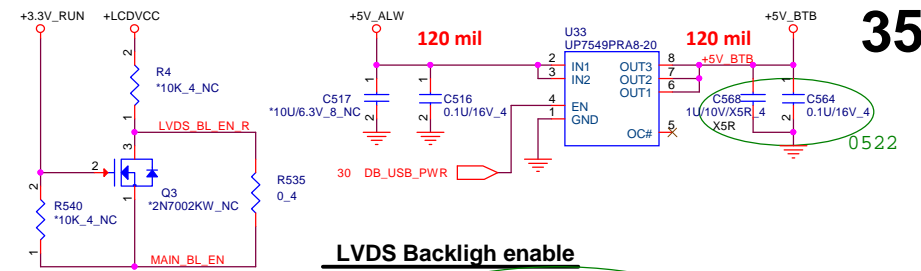
## Panel Count Application



### Panel SPEC

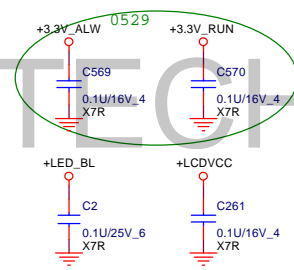
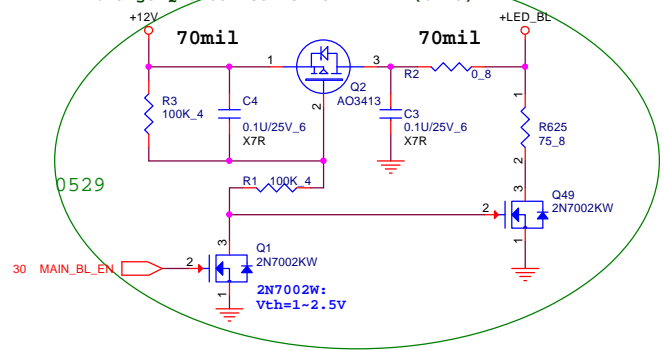
LCD Panel	LCDVCC		LED_BL	
	Vol.(V)	I (A)	Vol.(V)	I (A)
G121X1-L04 (12.1")	(1) 3.3 (2) 5.0	(1)0.65(max) (2)0.48(max)	12.0	0.5(max)
G150XGE-L04 (15)	3.3	0.69(max)	12.0	0.8(max)
LB170E01 (17")	5.0	1.16(max)	12.0	1.18(max)

NOTE : SPEC PGI14  
RTD2136N integrates a panel power switch for panel power control.  
The switch can support any panel resolution with the maximum current  
consumption below 1-A, and can endure panel inrush current up to 2-A

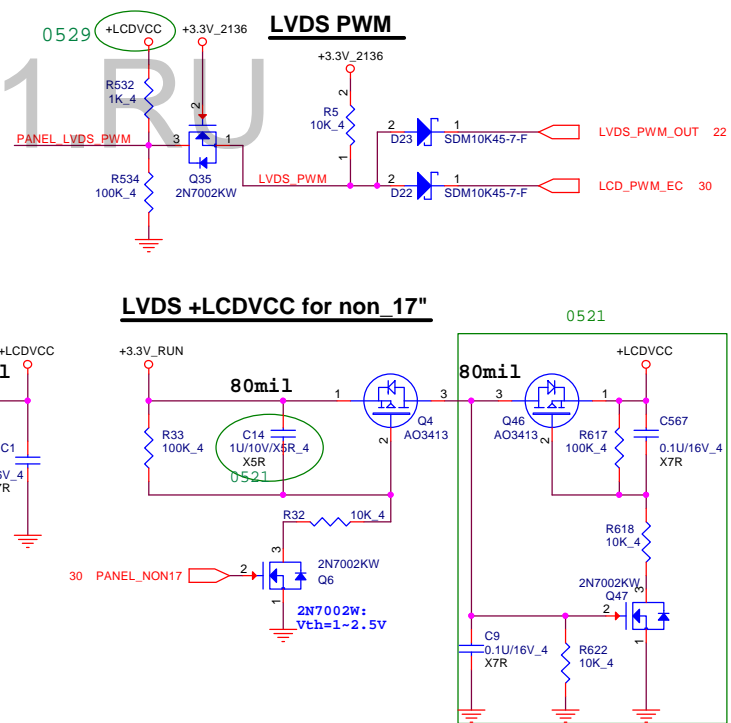
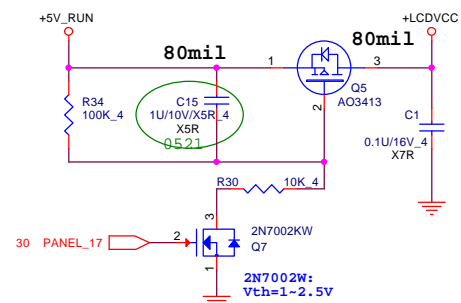


### LVDS Backligh enable

change Q10 to A03413 for BL=12V(0218)



### LVDS +LCDVCC for 17"



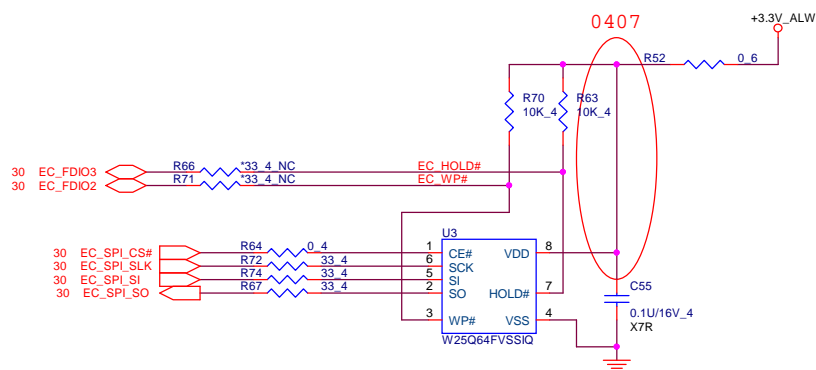
### LVDS +LCDVCC for non\_17"

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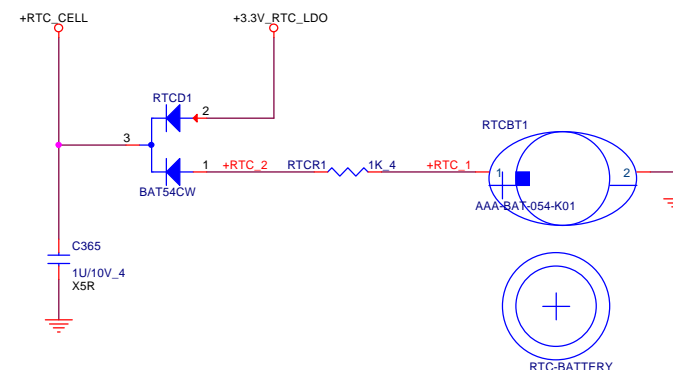
PROJECT : K97

Size	Document Number	Rev
	<b>Gold Finger</b>	1
Date:	Thursday, June 12, 2014	Sheet 35 of 51

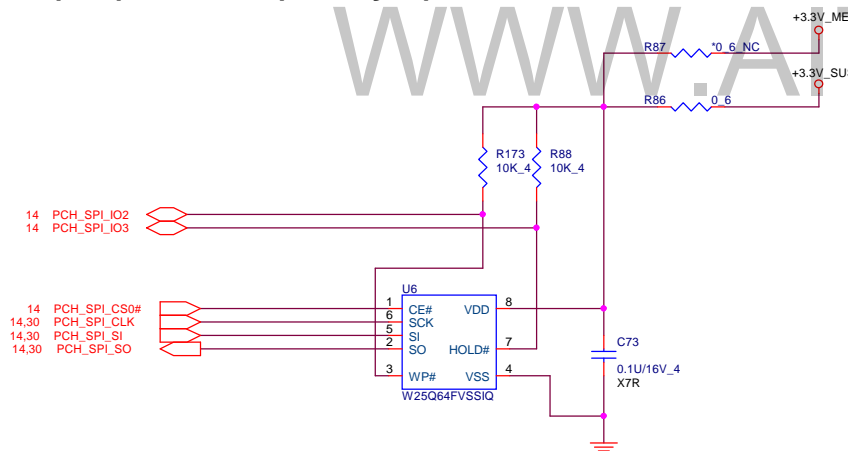
## For BIOS + EC + AMI Diag. 64Mbit (8M Byte)



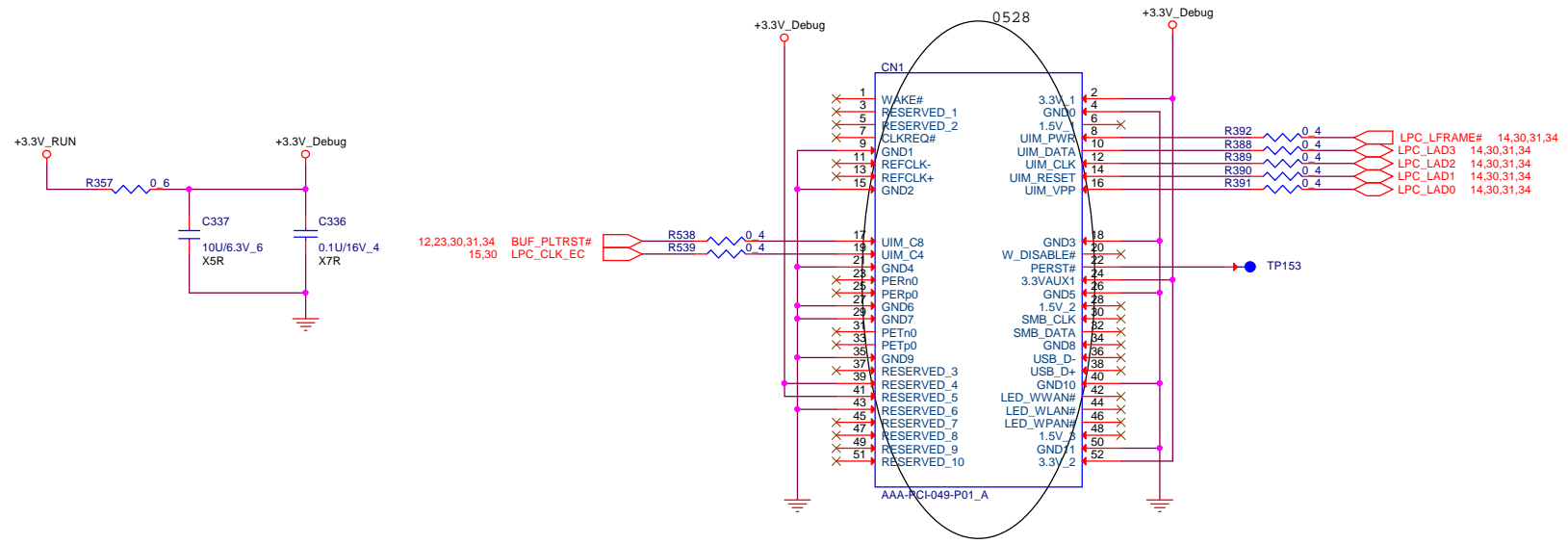
## RTC BATTERY



## For PCH(ME) 64Mbit (8M Byte)



SPI	H81 (2M)	Q87 (8M)	CS#
vPRO	NC	AKE3EFP0N07 (U6) IC FLASH(8P) W25Q64FVSSIQ(SOIC), 8M Note : only ME	CS0#
nonvPRO	AKE38FP0N03 (U6) IC FLASH(8P) W25Q16DVSSIQ (SOIC), 2M Note : only ME	NC	CS1#
EC	AKE3EFP0N07 (U3) IC FLASH(8P) W25Q64FVSSIQ(SOIC), 8M Note : BIOS + EC + AMI Diag.	AKE3EGN0Q01 (U3) IC FLASH(8P)GD25B64BSIGR(SOP)8M Note : BIOS + EC + AMI Diag.	CS1#

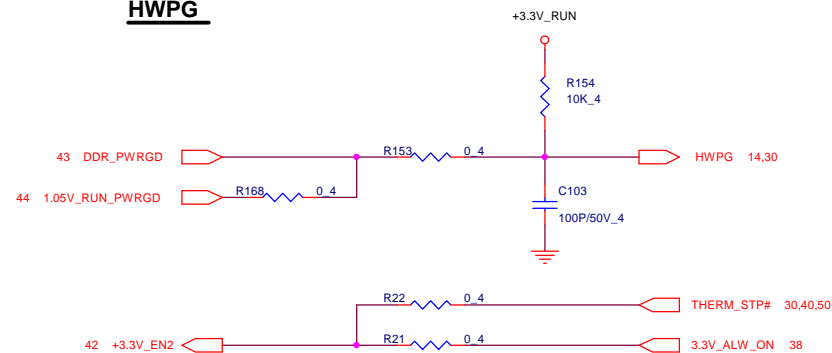


WWW.AITECH1.RU



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**HWPG**

Finger print	5V	120mA
I-button	5V	90mA
MSR1	5V	5mA
MSR2	5V	100mA
RFID	5V	130mA

WWW.AITECH1.RU



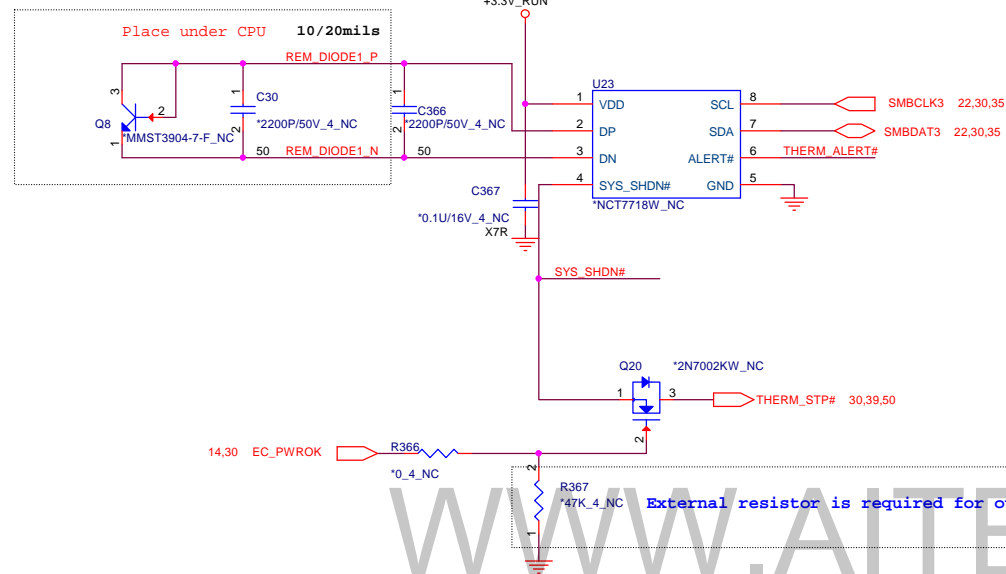
**Quanta Computer Inc.**

**PROJECT : K97**

Size	Document Number	Rev
		1A
Date:	Thursday, June 12, 2014	Sheet 39 of 51

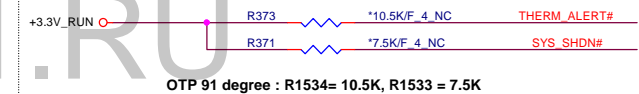
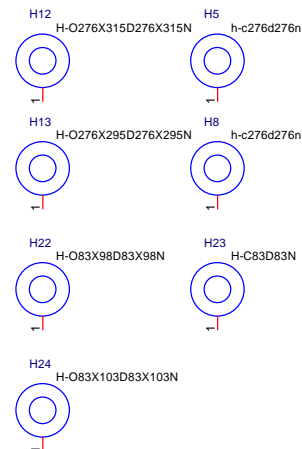
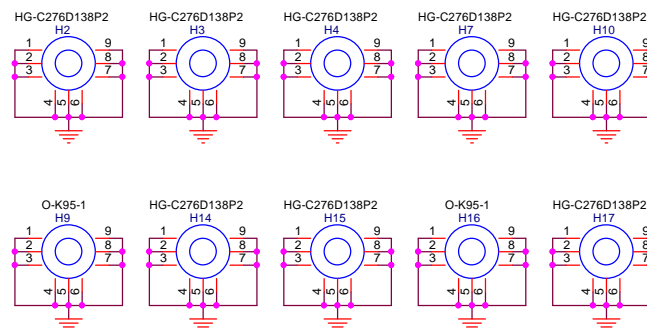
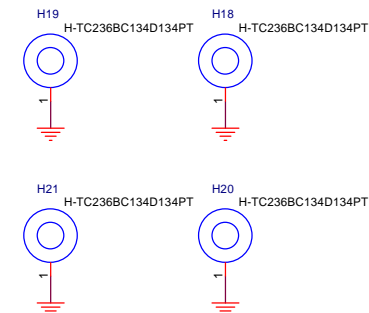
**THERMAL IC**

Need closed to CPU



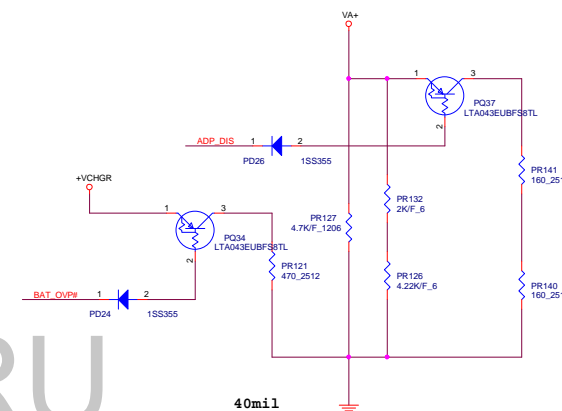
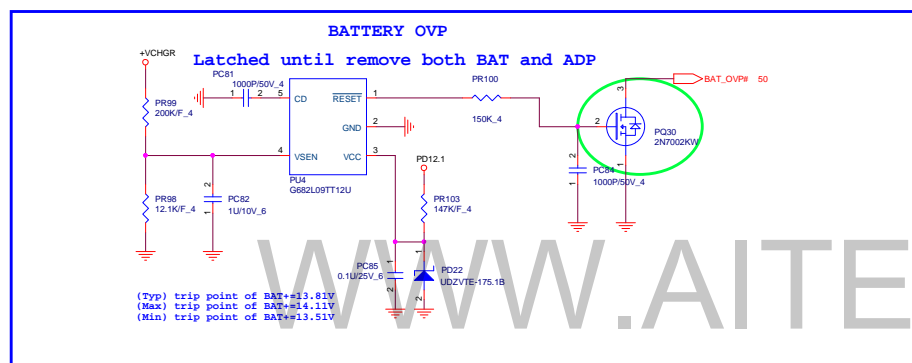
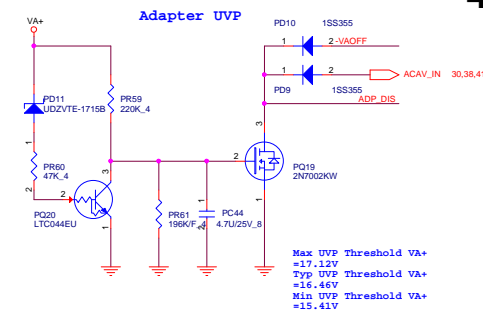
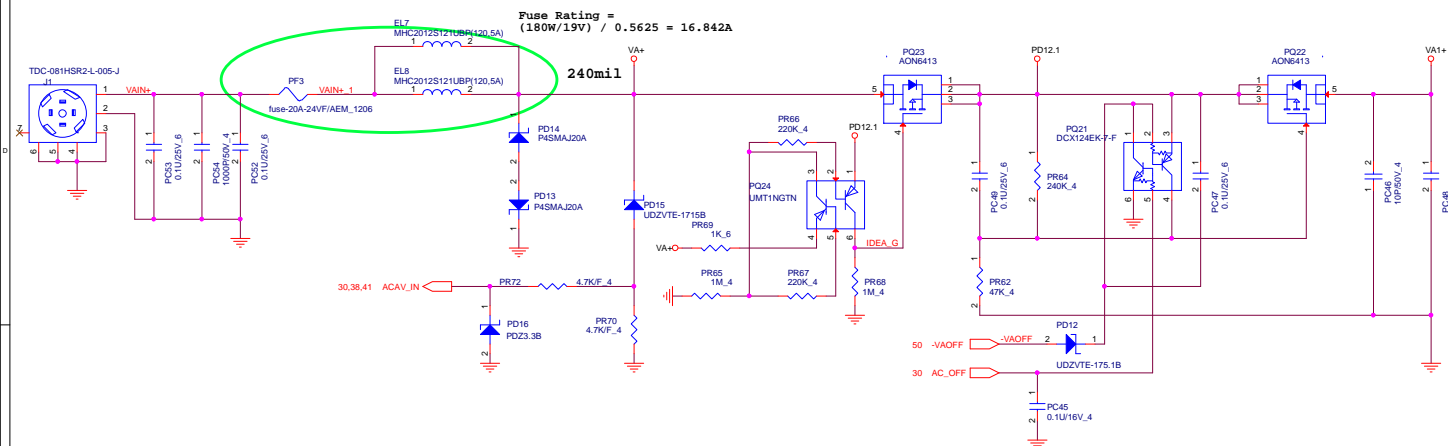
SYS_SHDN#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77 'C	87 'C	97 'C	107 'C	117 'C
7.5K	79 'C	89 'C	99 'C	109 'C	119 'C
10.5K	81 'C	91 'C	101 'C	111 'C	121 'C
14K	83 'C	93 'C	103 'C	113 'C	123 'C
18.7K	85 'C	95 'C	105 'C	115 'C	125 'C

OTP 91 degree C

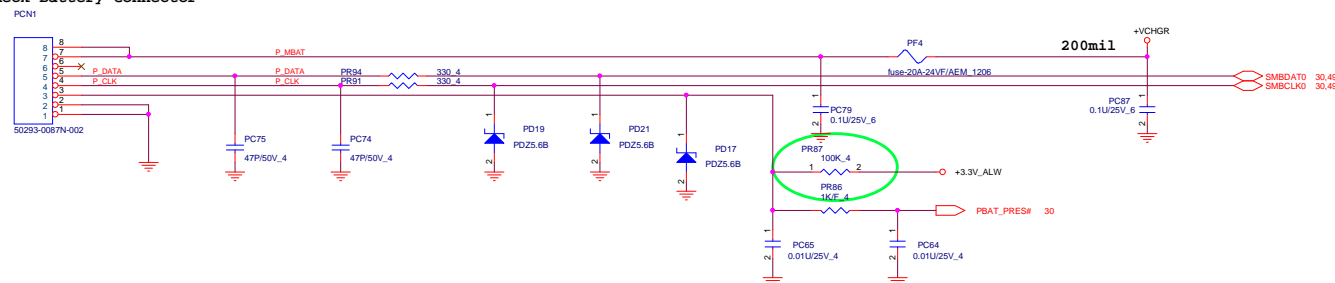
**ME HOLE****MB HOLE****Thermal HOLE**

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**PROJECT : K97**

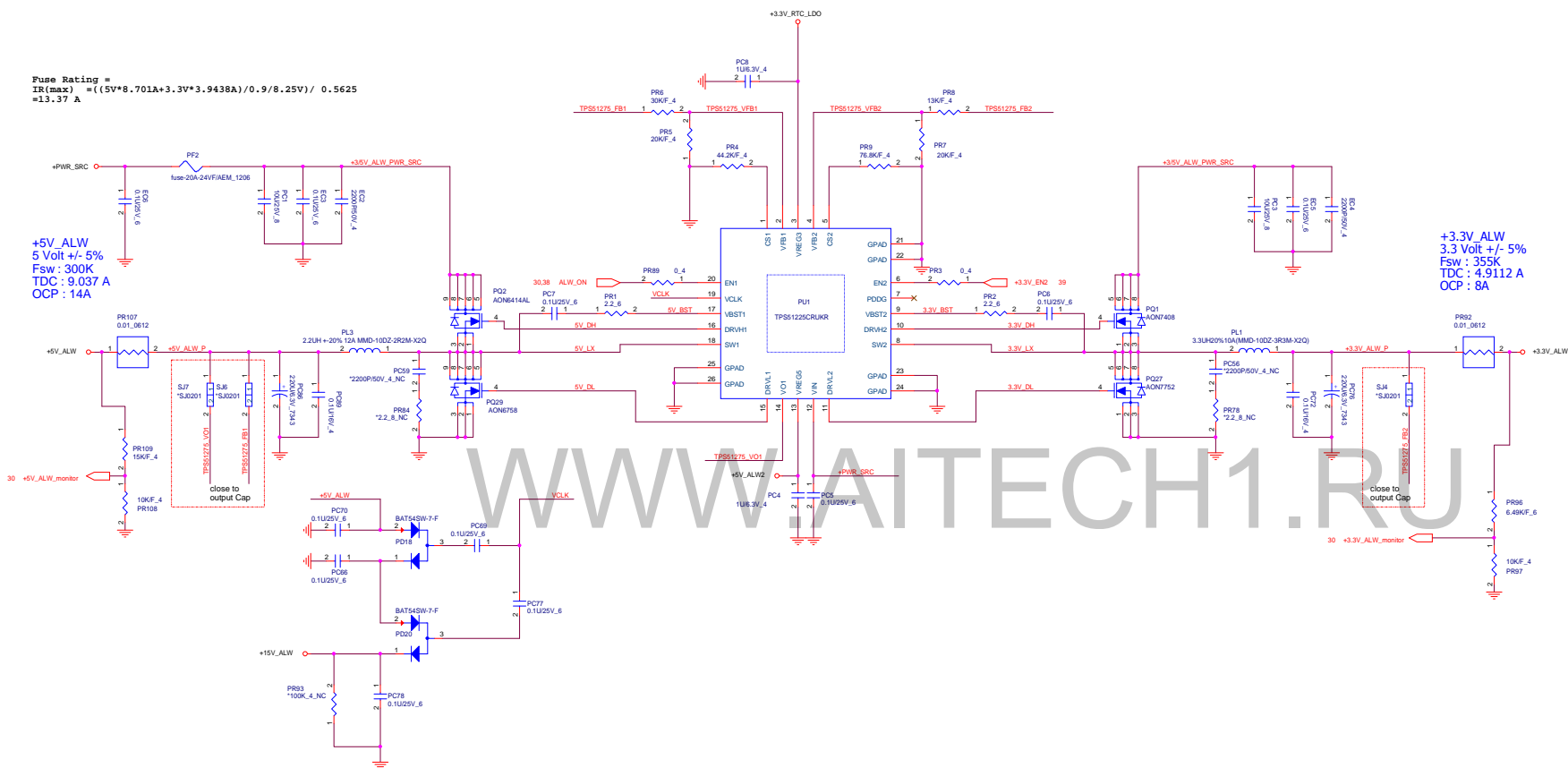


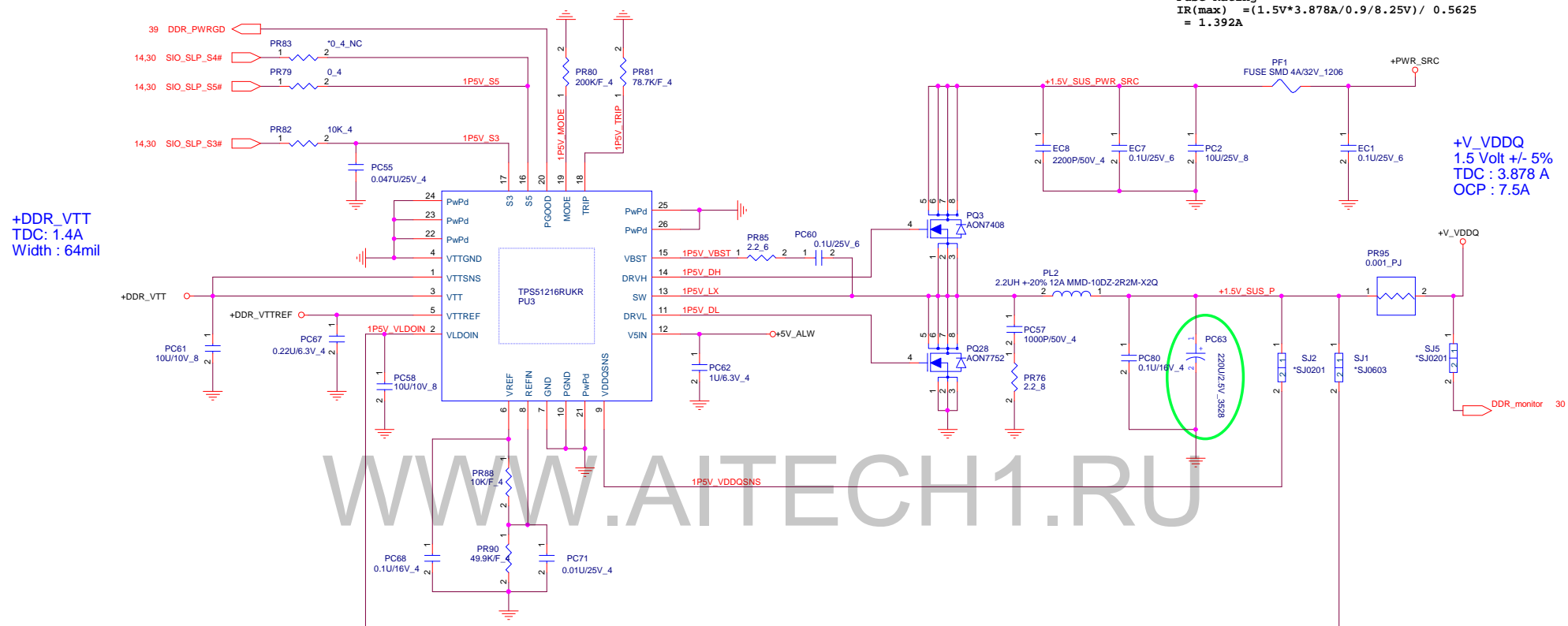


Need check Battery Connector



Fuse Rating =  
 $I_R(max) = ((5V \cdot 8.701A + 3.3V \cdot 3.9438A) / 0.9 / 8.25V) / 0.5625$   
 = 13.37 A





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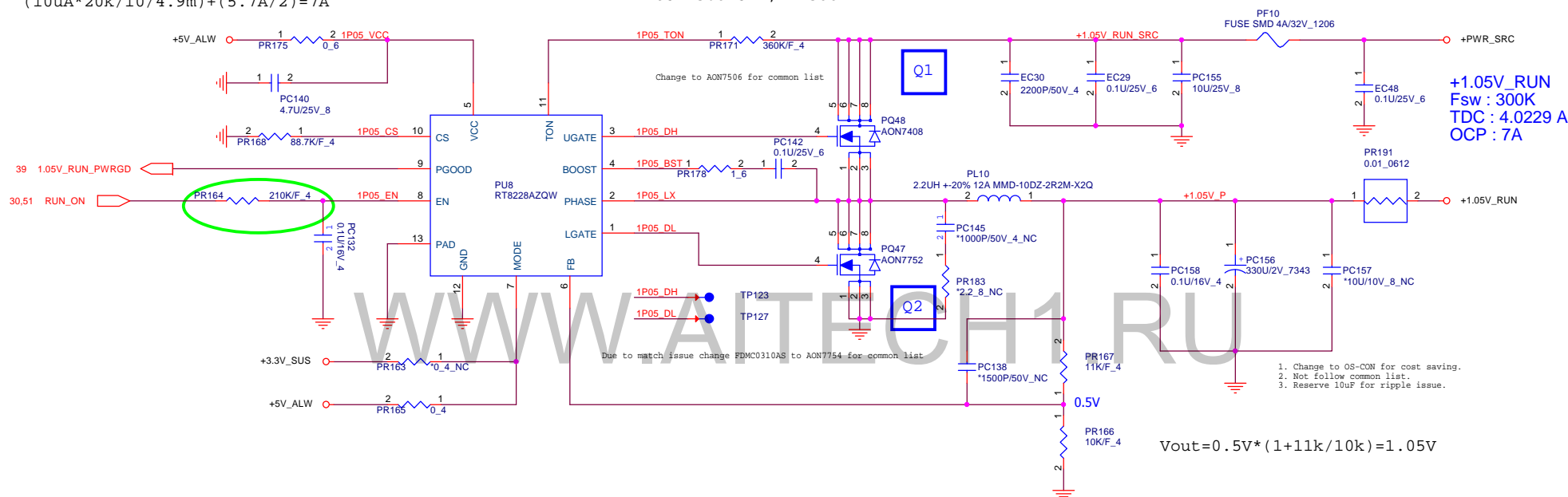
**PROJECT : K97**

Size	Document Number	Rev
	<b>DDR3L (TPS51216RUKR)</b>	<b>1A</b>
Date:	Thursday, June 12, 2014	Sheet 43 of 51

$$OCP = \text{Current limit} + I_{\text{ripple}}/2 = (10\mu A * 20k/10/4.9m) + (5.7A/2) = 7A$$

$$R_{\text{ton}} = 360k\Omega, F = 300KHz$$

$$\text{Fuse Rating} = IR(\text{max}) = (1.05V * 4.0229A / 0.9 / 8.25V) / 0.5625 = 1.011A$$

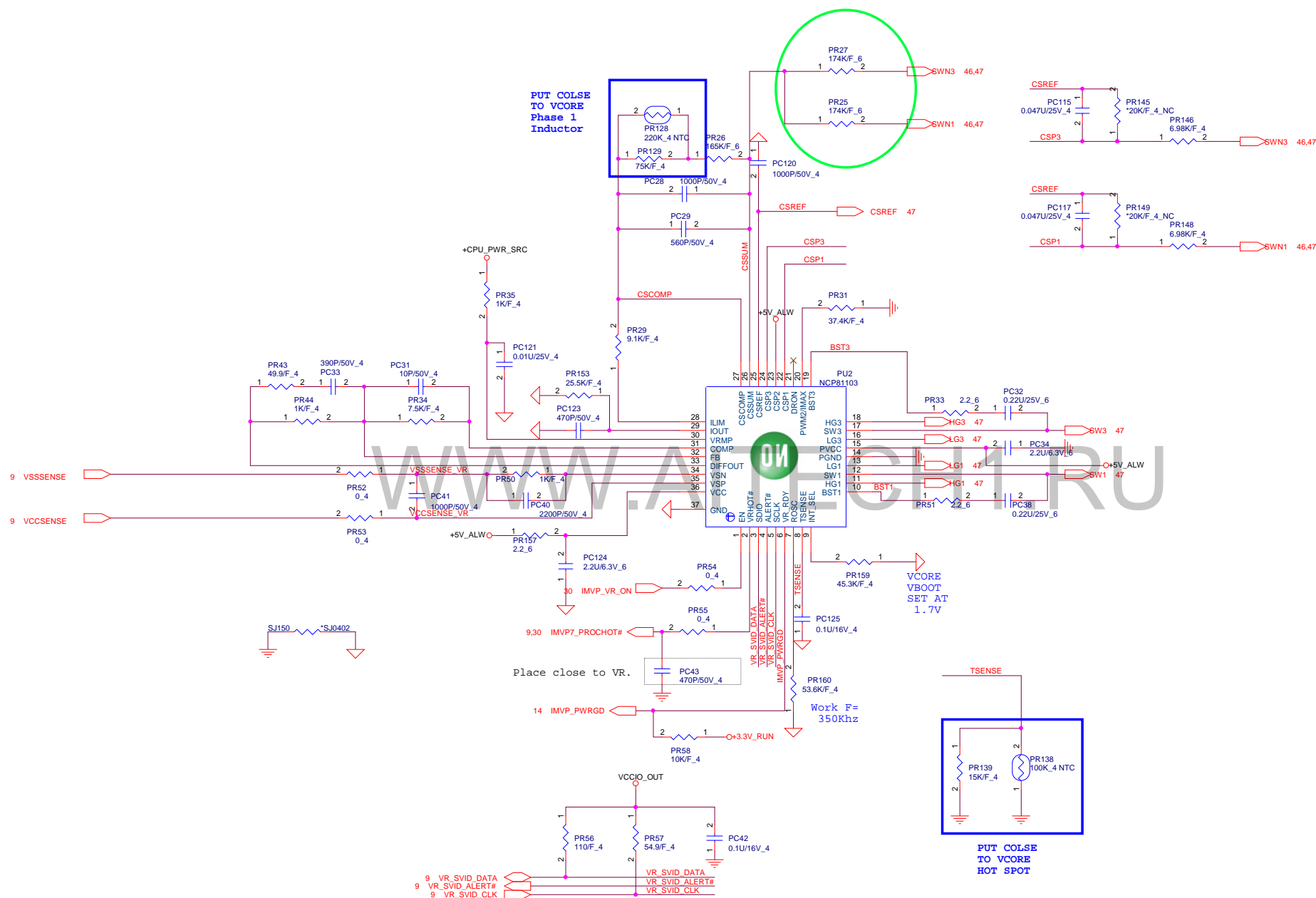


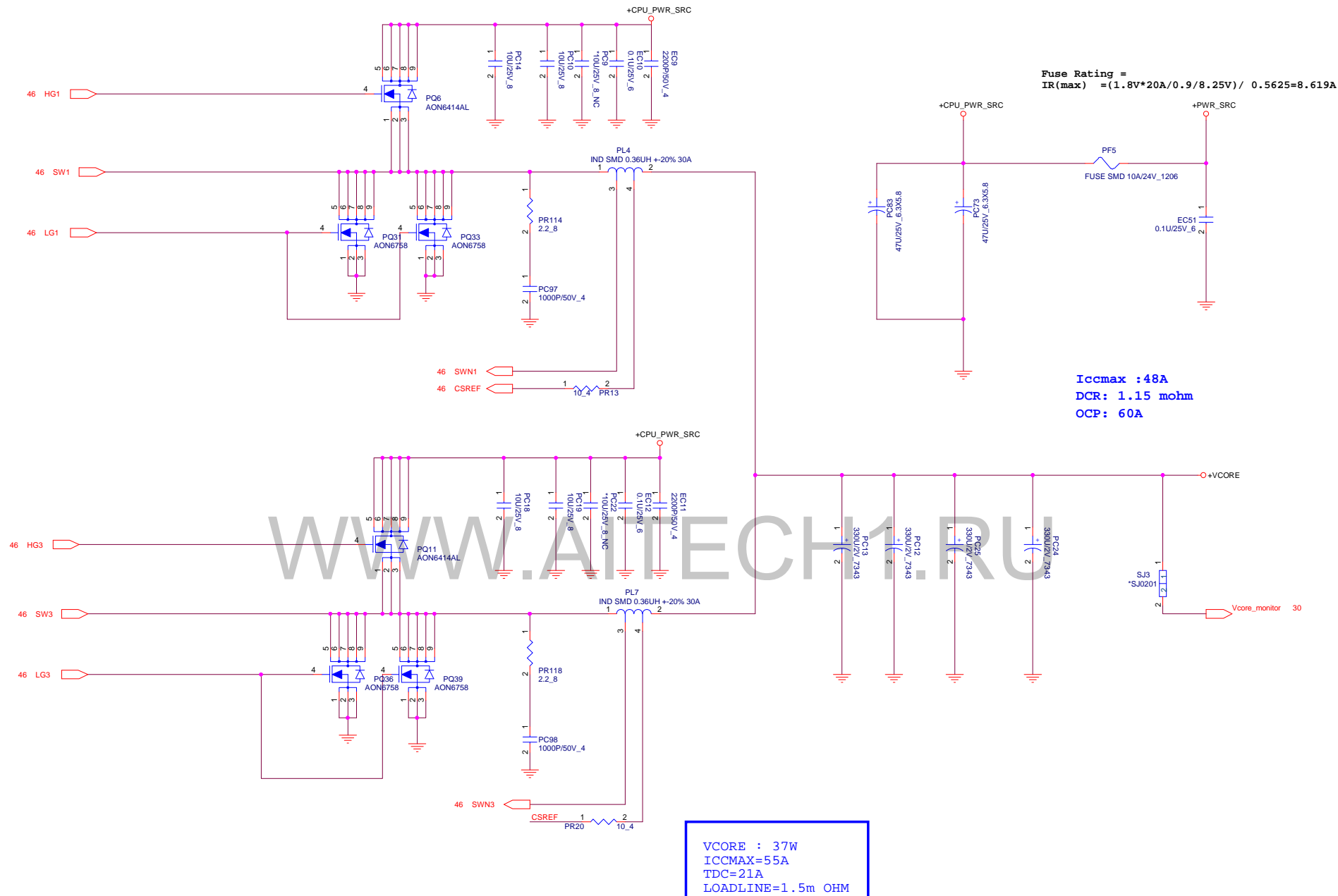
**Quanta Computer Inc.**

**PROJECT : K97**

Size	Document Number	Rev
	<b>1.05V_RUN (RT8228AZ)</b>	<b>1B</b>
Date:	Thursday, June 12, 2014	Sheet 44 of 51







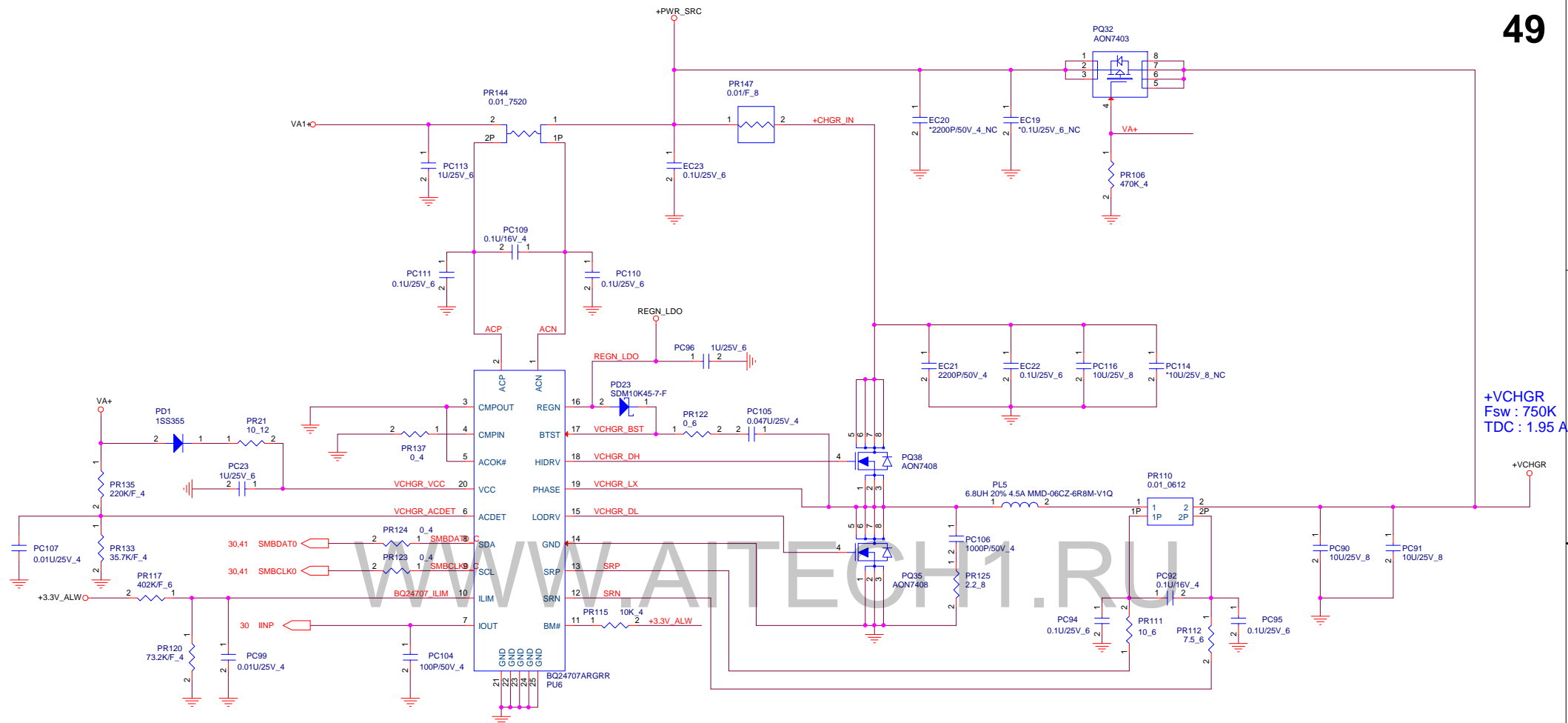
Quanta Computer Inc.

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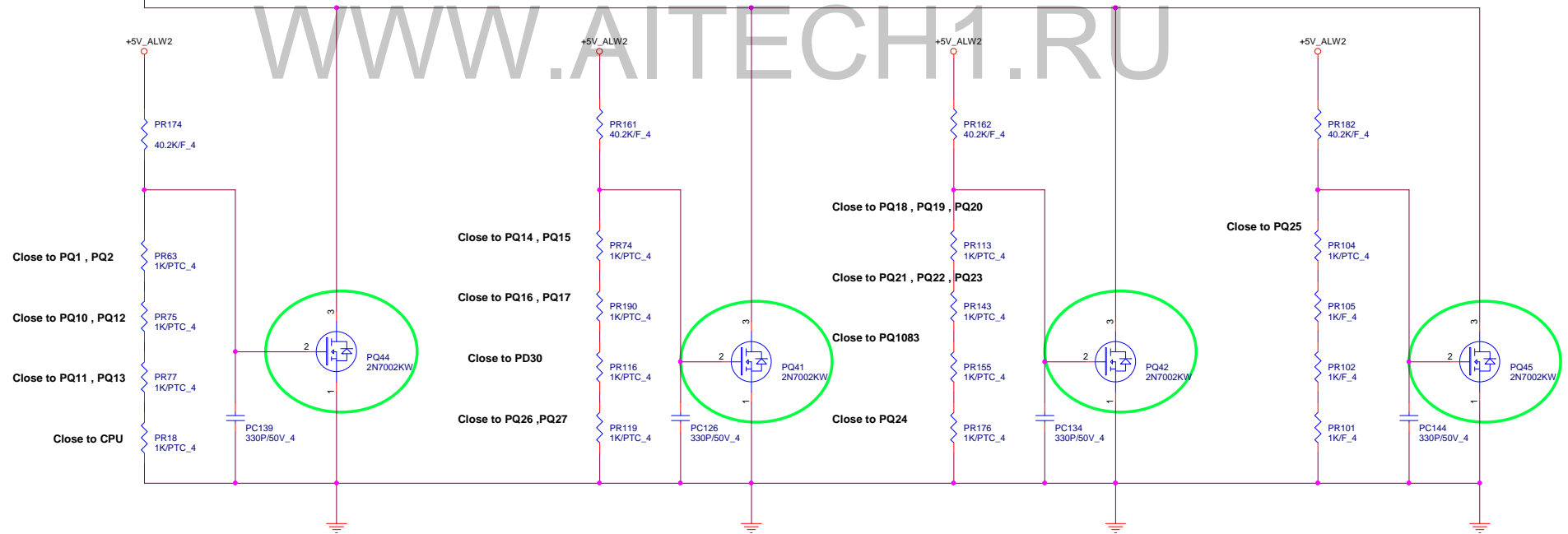
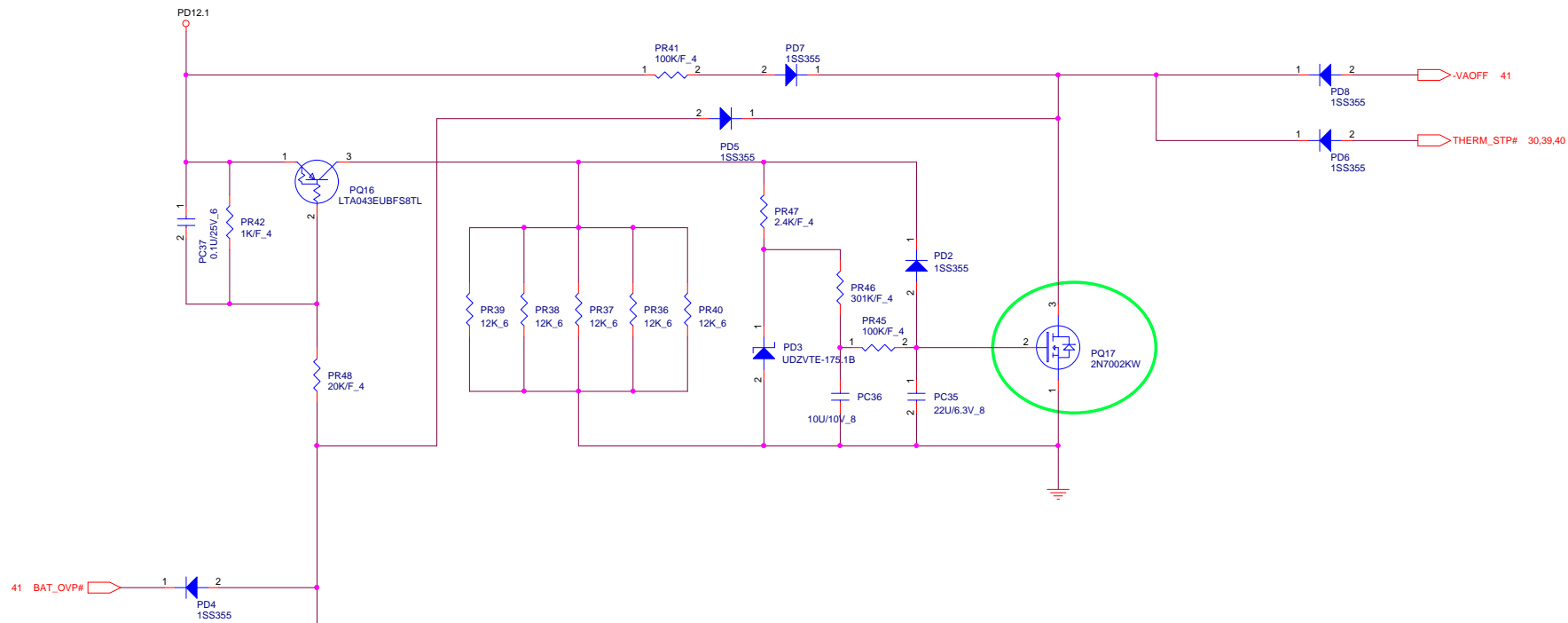
Size	Document Number	Rev
	CPU_CORE(NCP81103 Stage)	A0
Date:	Thursday, June 12, 2014	Sheet 47 of 51

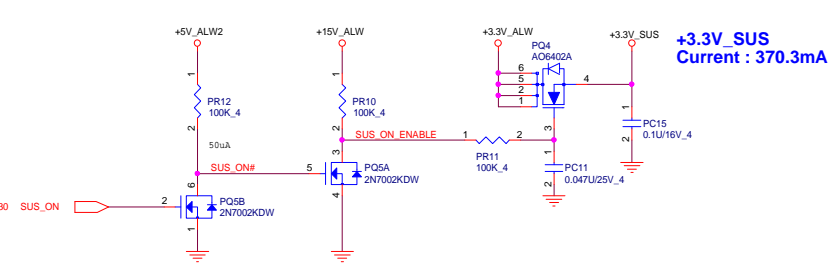
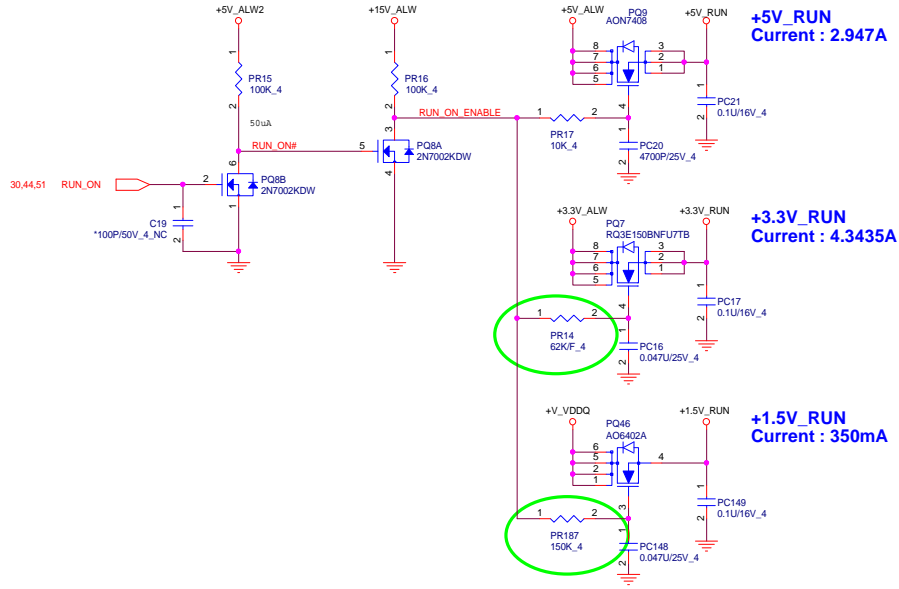
4





```
Adapter type : 180W
Battery: 3S1P (8.25V)
Charge Current Limit Set to 2.5 A
```



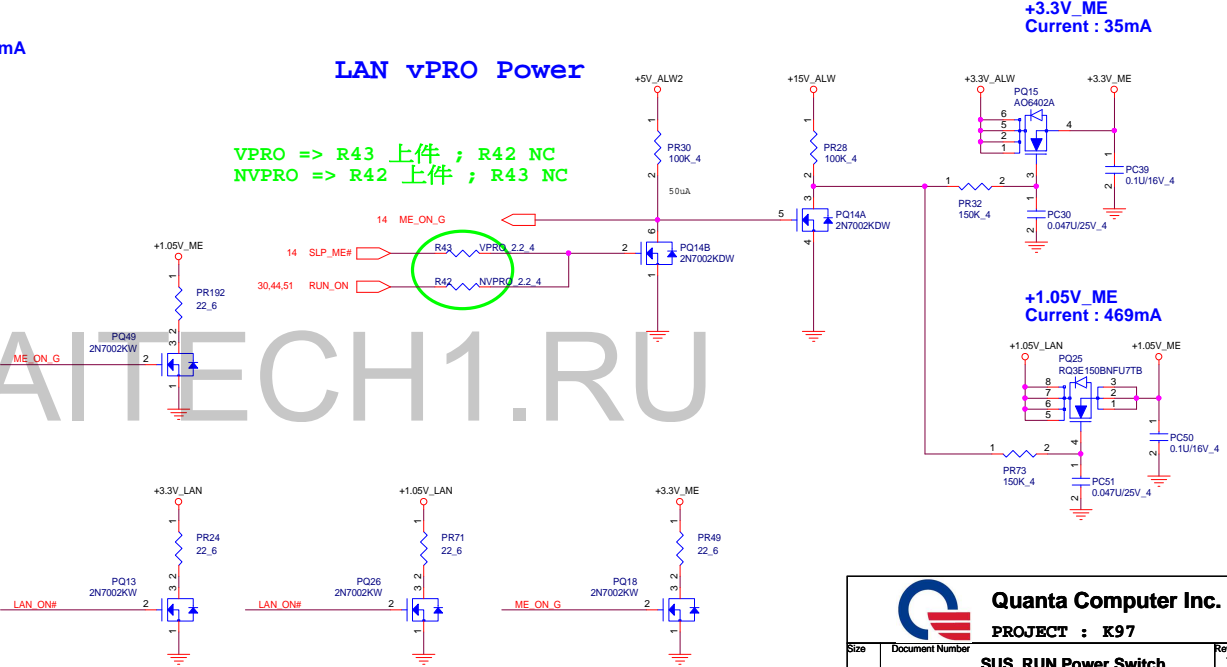
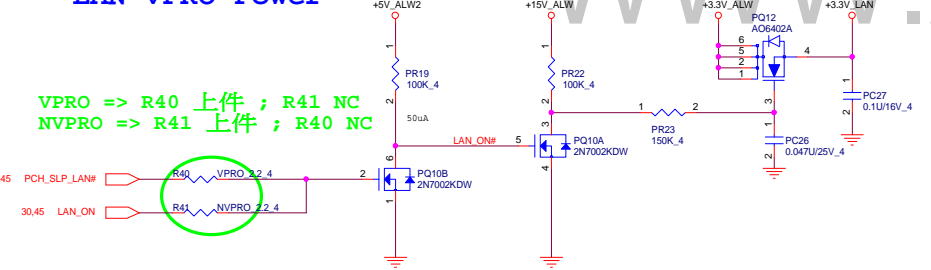



LAN vPRO Power

VPRO => R43 上件 ; R42 NC  
NVPRO => R42 上件 ; R43 NC

LAN vPRO Power

VPRO => R40 上件 ; R41 NC  
NVPRO => R41 上件 ; R40 NC



		<b>Quanta Computer Inc.</b>	
		<b>PROJECT : K97</b>	
Size	Document Number	<b>SUS_RUN Power Switch</b>	
Date: Thursday, June 12, 2014		Sheet	51 of 51